



Layout : Q87/B85H3-AM co-lay  
Schematic: Q87 only  
Rev:1.0

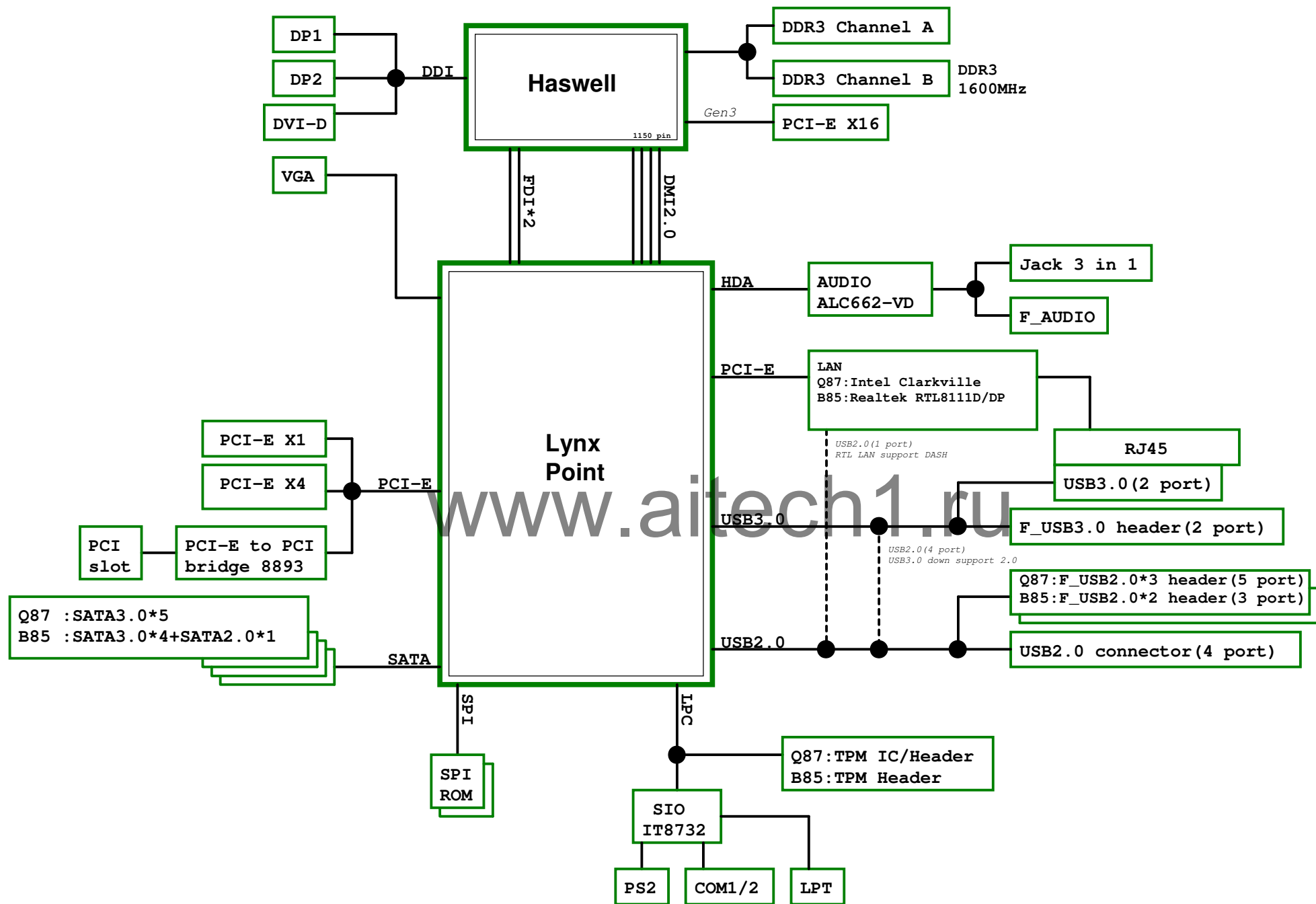
ECS  
CONFIDENTIAL

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REVISION HISTORY:

Rev	Date	Notes
27		ECIO-IT8732
28		FAN/PS2/Buzzer/F_Panel
29		LPT/COM/TPM
30		LAN Intel & Realtek
31		LAN+USB3.0 Connector
32		AUDIO-ALC662_VD
33		AUDIO-CONN & Header
34		XDP-CPU/PCH
35		DC/DC VDIMM/DDR_VTT/5VDUAL
36		DC/DC PCH_1.5V/PCH,ME_1.05V
37		DC/DC ATX_3VSB/3VDUAL
38		DC/DC Vcore /Gate driver
39		DC/DC VCC3 & VCC & ATX12P
40		PWR Delivery
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42		CLK Distribution



## PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO13	3VSB	LPC_PME	GPI
GPIO24	3VSB	USB_5VDUAL control (reserve)	GPO
GPIO72	3VSB	USB_5VDUAL control	Native
GPIO45	3VSB	BIOS WP	Native
GPIO57	3VSB	BIOS WP	GPI
GPIO46	3VSB	WLAN_DIS_L	Native
GPIO61	3VSB	LPCPD_L	Native
GPIO27	ATX_3VSB	ILAN_WAKE_L	GPI
GPIO1	VCC3	OBR	GPI
GPIO6	VCC3	Thermal_SD	GPI
GPIO68	VCC3	TP_VGA	GPI
GPIO23	VCC3	HDPANEL_DETECT	Native
GPIO15	3VSB	PEX16_RST	GPO
DL, BIOS must be pro			
GPIO73	3VSB	case open(reserve)	PCIECLKRQ0#
GPIO14	3VSB	ME_Disable	Native
GPIO19	VCC3	BOOT device detect	GPI
GPIO51	VCC3	BOOT device detect	GPO

## Interrupt mapping

Function	INT# port	PCIe*1 port	Device
PCI Bridge	INTA#	port 1	IC IT8893
mini-PCIE	INTB#	port 2	LPT integrate
LAN	INTC#	port 3	Clarkville or RTL8111DP
PCIEX1	INTD#	port 4	LPT integrate
PCIEX4	INTA#/B#/C#/D#	port 5~8	LPT integrate
SATA	INTB#	NA	LPT integrate

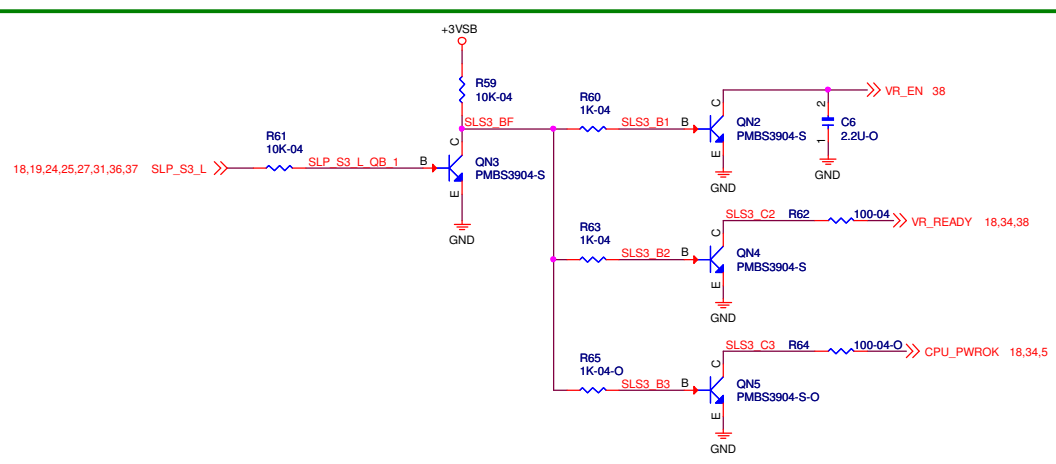
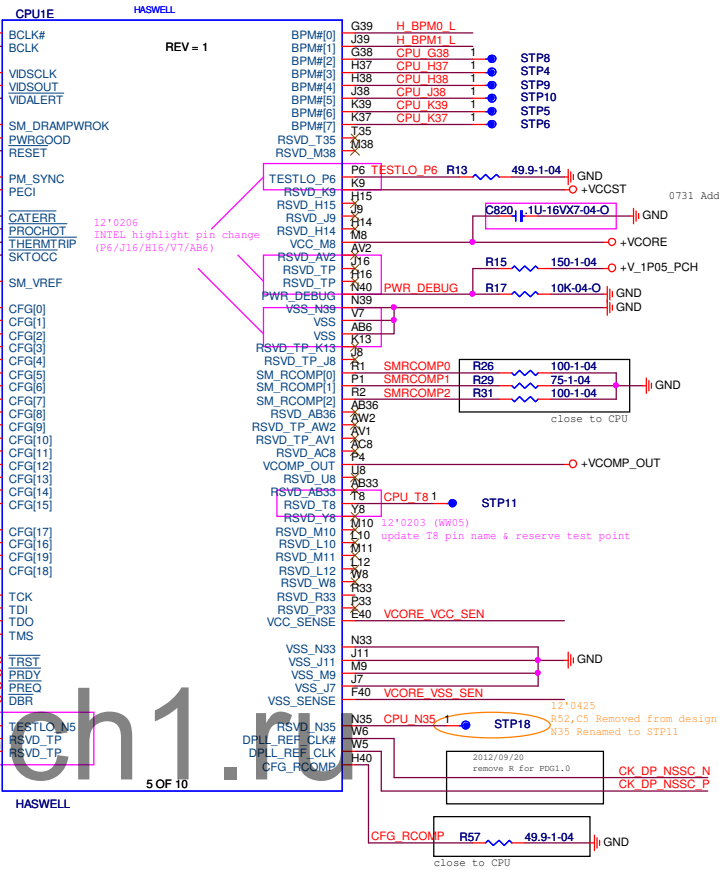
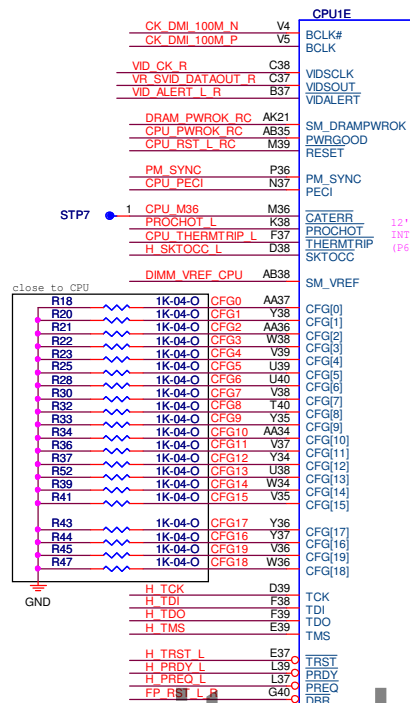
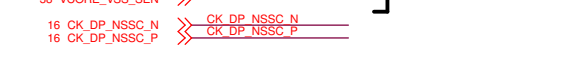
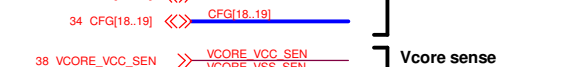
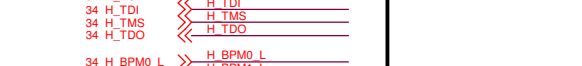
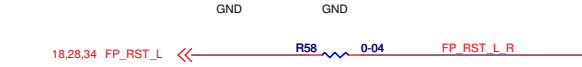
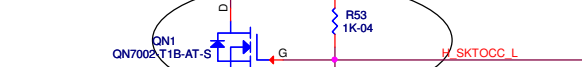
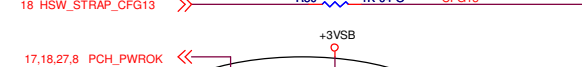
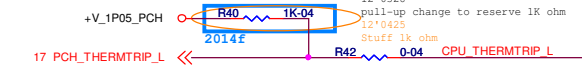
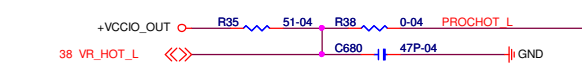
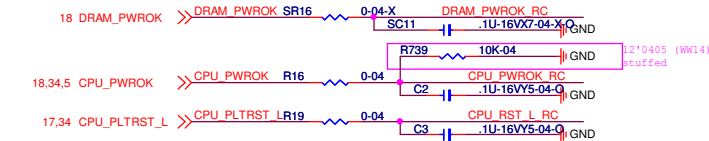
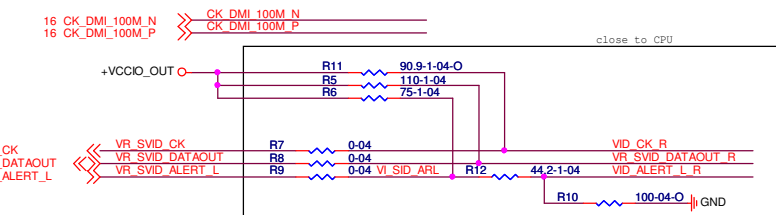
## SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP16	VCC3	Beep(reserve)	CIRR2
GP36	3VSB	Thermal_SD	FAN_CTL3
These GPIO pins are kept by VCC in default but can be changed to be kept by 3VSB if EC side writes 1 to 2012h[bit 5].			
GP35	3VSB	LED0	FAN_TAC4
GP37	3VSB	LED1	FAN_TAC3
GP70	VCC3	TPM Onboard detect	GPI
GP71	VCC3	BOM detect	GPI
GP73	VCC3	BOM detect	GPI
GP74	VCC3	BOM detect	GPI
GP76	VCC3	Thermal_HD_Auto_Switch	GPI
GP46	3VSB	Acer Header	GPI
GP47	3VSB	Acer Header	GPI
GP40	3VSB	5VDUAL Switch	3VSB

BIOS must be pro to Native 3VSB

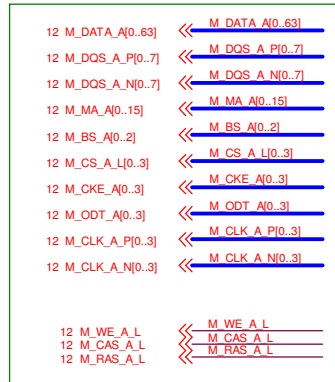




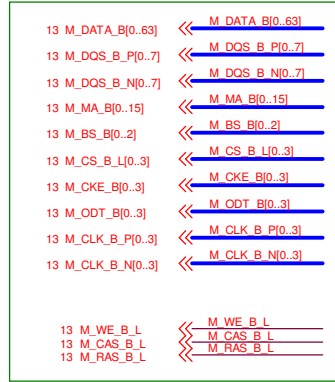


# Power Down Sequencing Circuit

Title			CPU-MISC
Size	Custom	Document Number	Q87H3-AM
Date:	Thursday, March 28, 2013	Sheet	5 of 42
Rev	1.0		



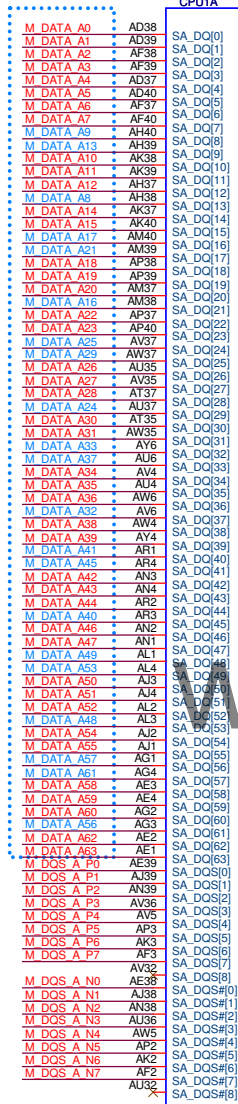
DDR3 CH.A



DDR3 CH.B

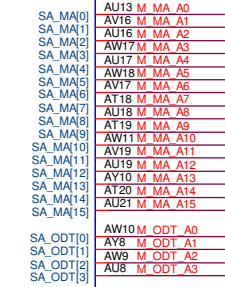
12,13,6 DDR3\_DRAMRST\_L << DDR3\_DRAMRST\_L

\*\*Attention



CPU1A HASWELL

REV = 1



RSVD\_AW12

TP12

SA\_RAS

SA\_WE

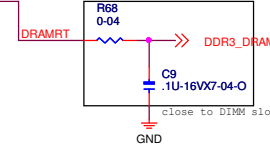
RSVD\_AW20

RSVD\_AW27

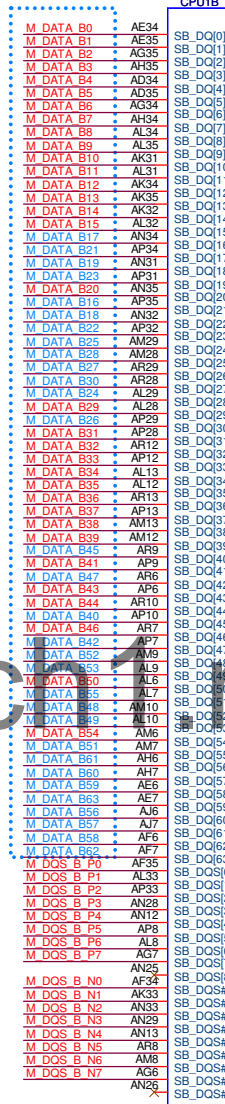
SA\_CAS

SM\_DRAMRST

1 OF 10

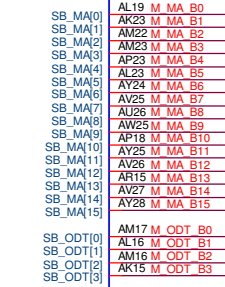


\*\*Attention



CPU1B HASWELL

REV = 1



RSVD\_AL20

SB\_CAS

RSVD\_AL20

SB\_RAS

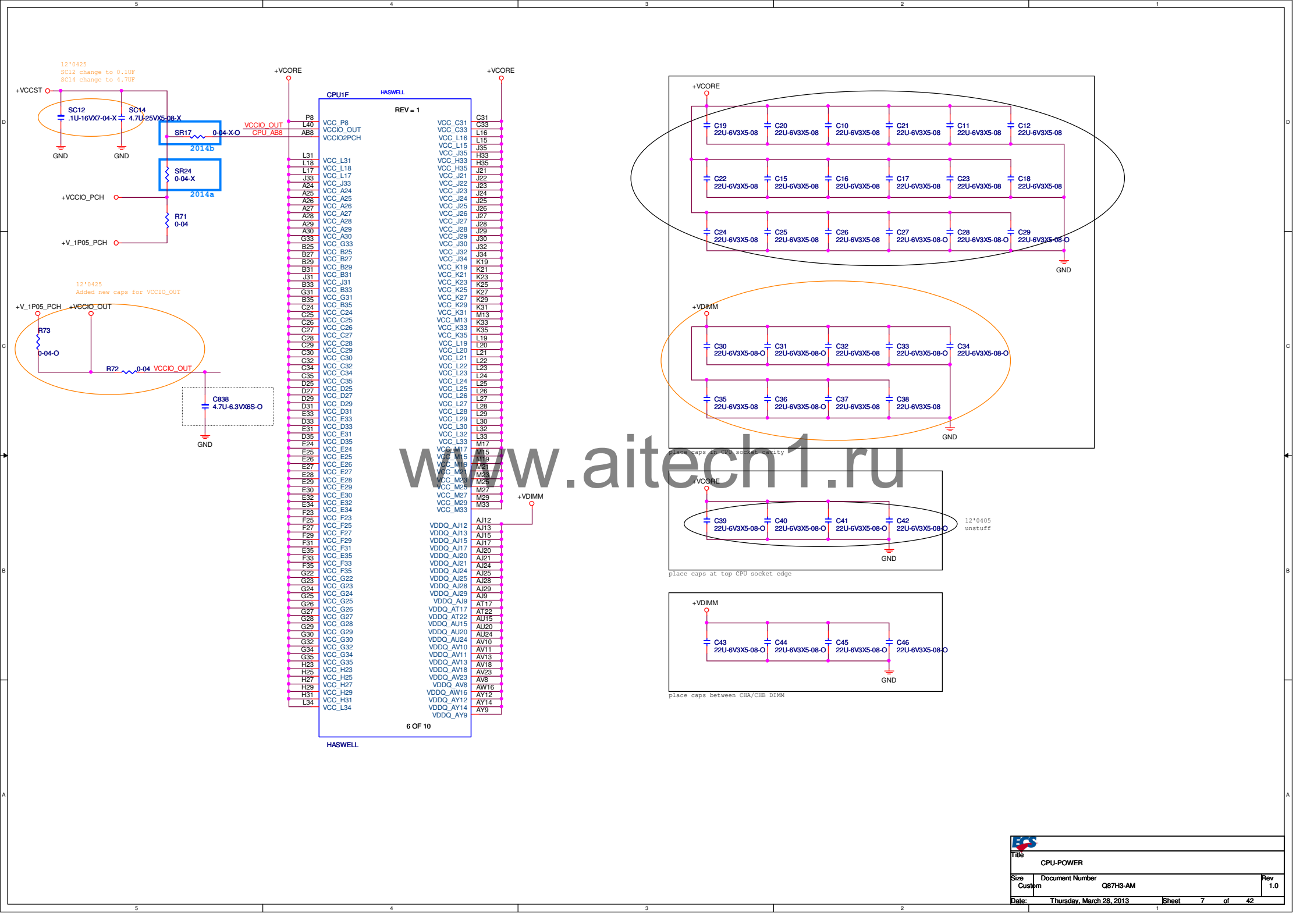
SB\_WE

SA\_DIMM\_VREFDQ

SB\_DIMM\_VREFDQ

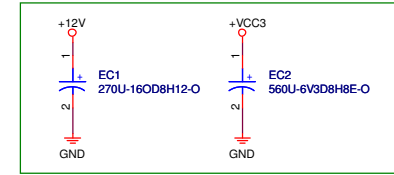
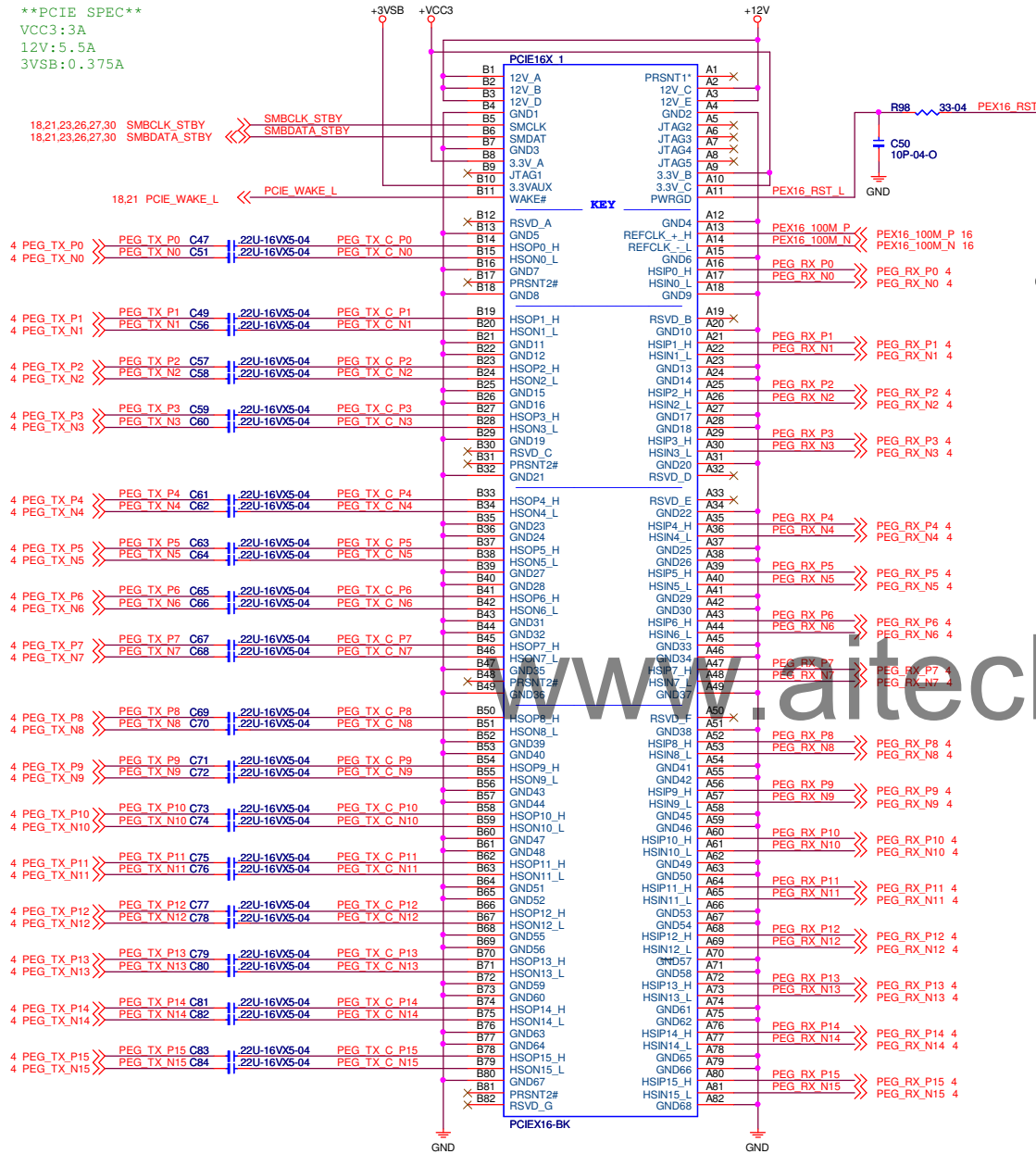
1 OF 10

2 OF 10

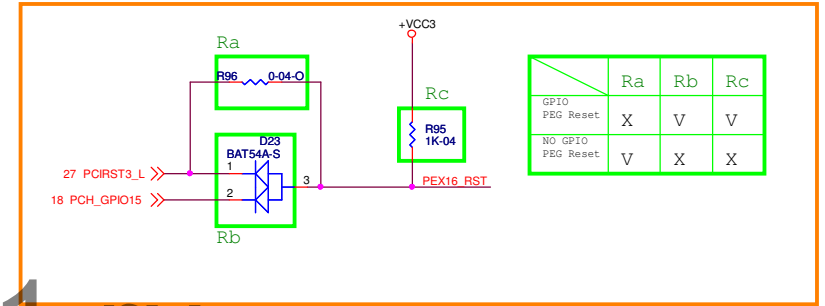
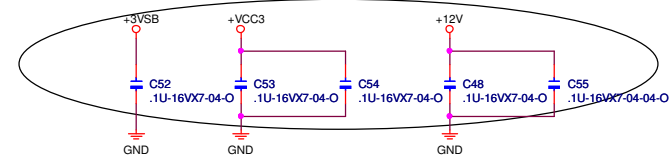




\*\*PCIE SPEC\*\*  
VCC3: 3A  
12V: 5.5A  
3VSB: 0.375A



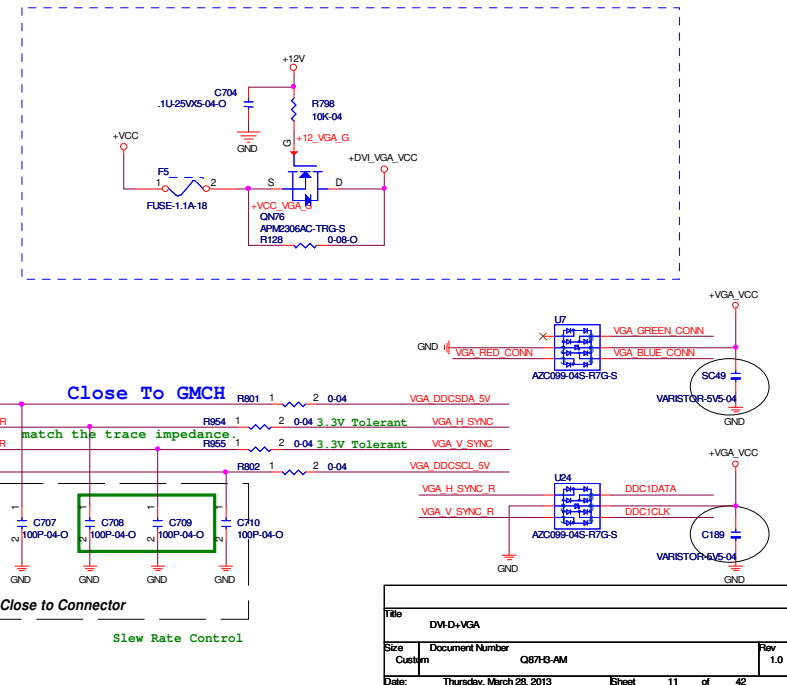
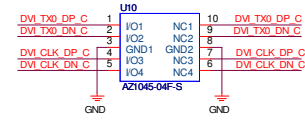
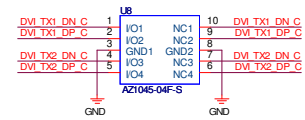
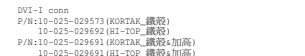
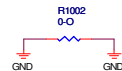
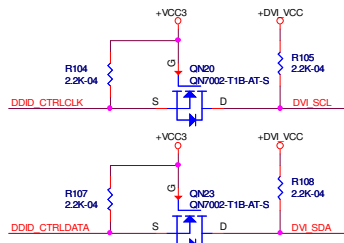
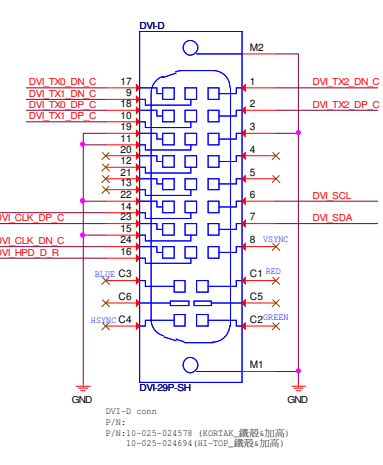
Between PCIe16 & PCIe1



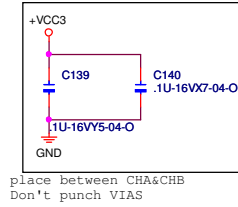
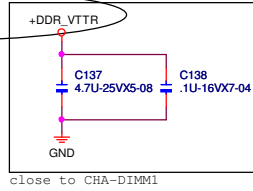
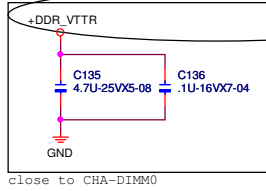
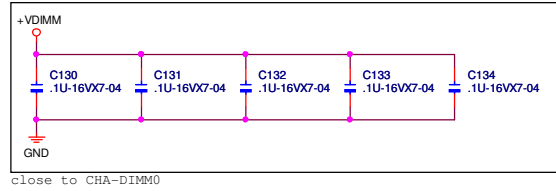
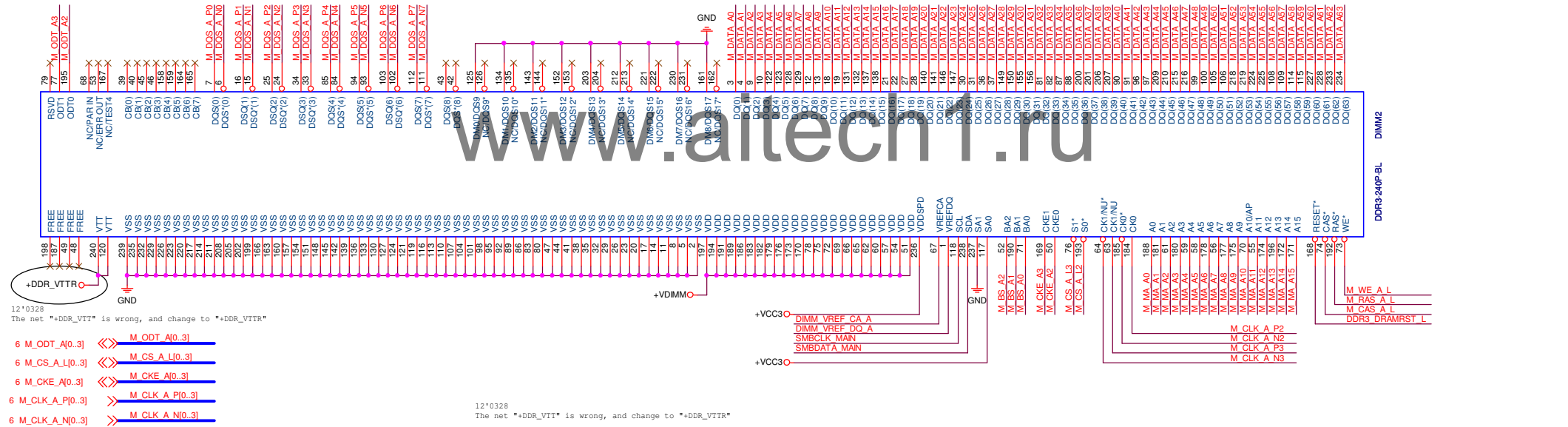
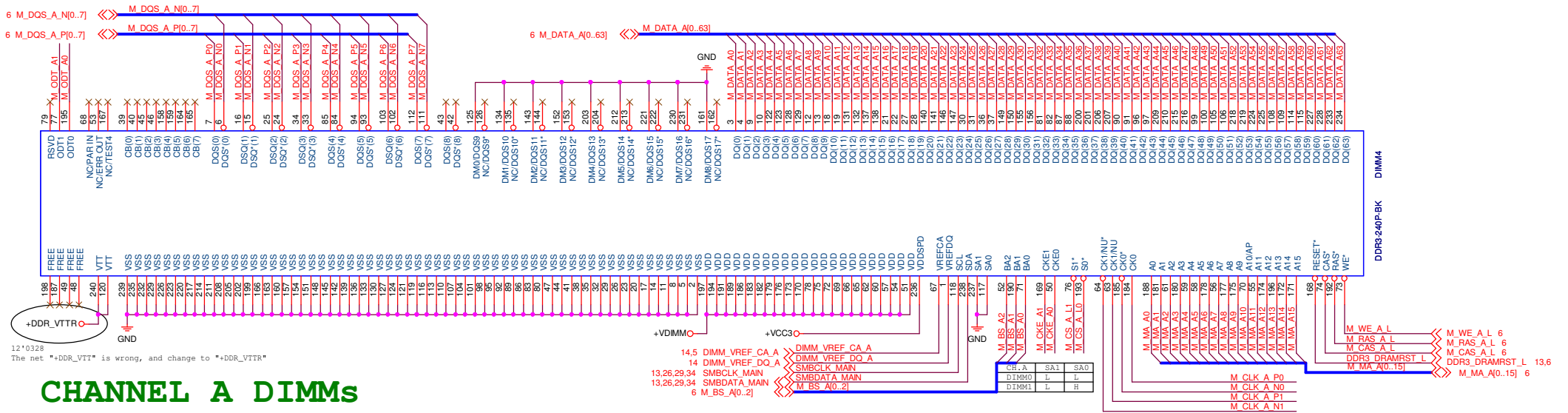
2012/7/05  
PCIe Gen3 slot reset circuit update .





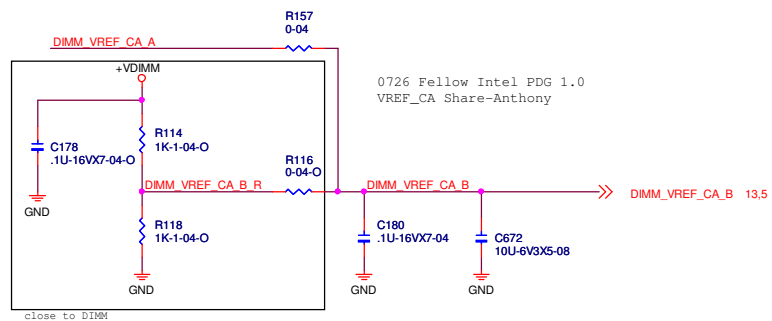
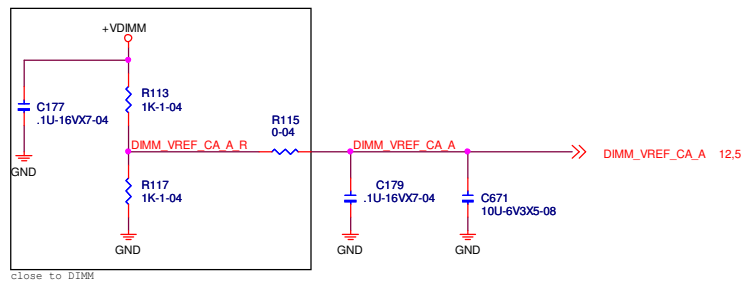


				GND	
Title					
DVI-D+VGA					
Size	Document Number				Rev
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Date:	Thursday, March 28, 2013		Sheet	11	of 42

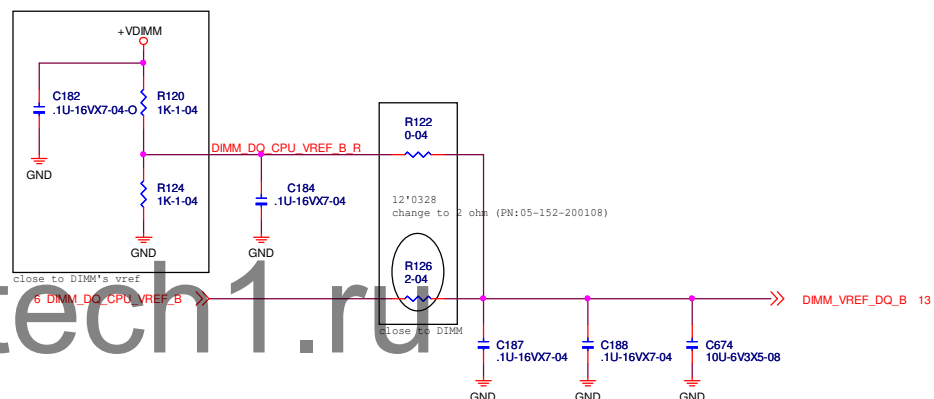
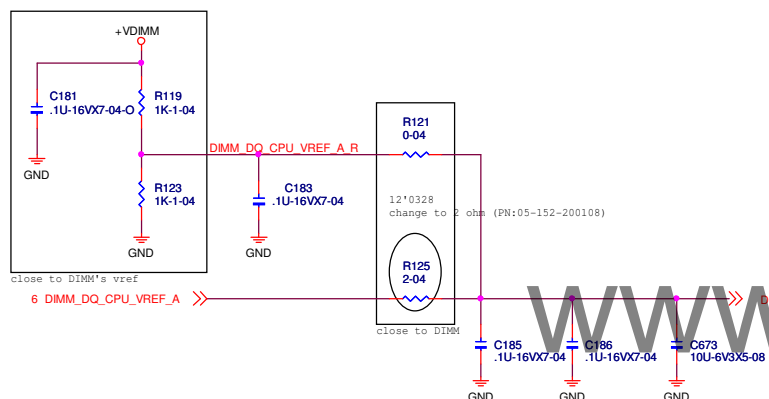




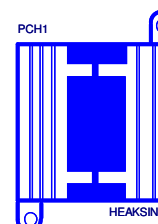




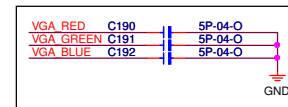
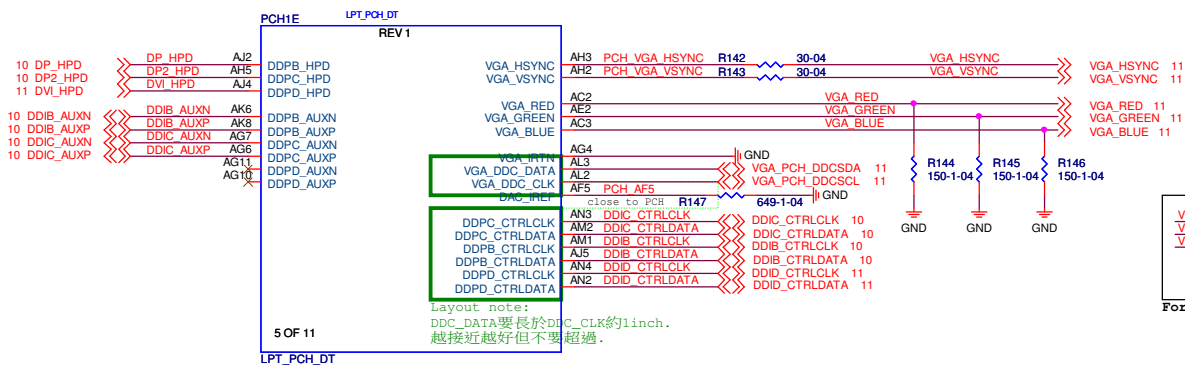
**DIMM\_VREF\_CA Circuit**



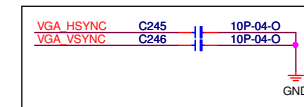
**DIMM\_VREF\_DQ Circuit**



PCH chipset (SMD)  
P/N:01D201-082640



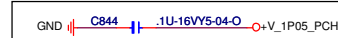
For EMI, close to chipset.



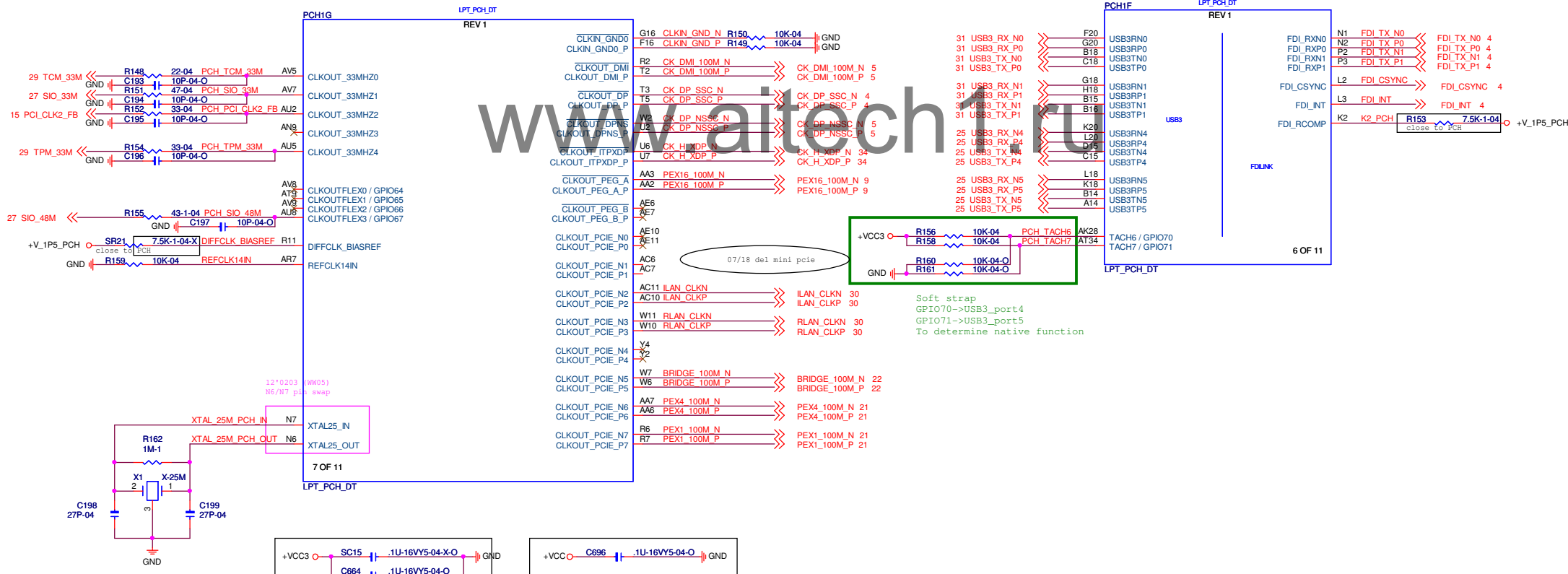
2012/07/09  
 Reserved Cap for Slew rate control

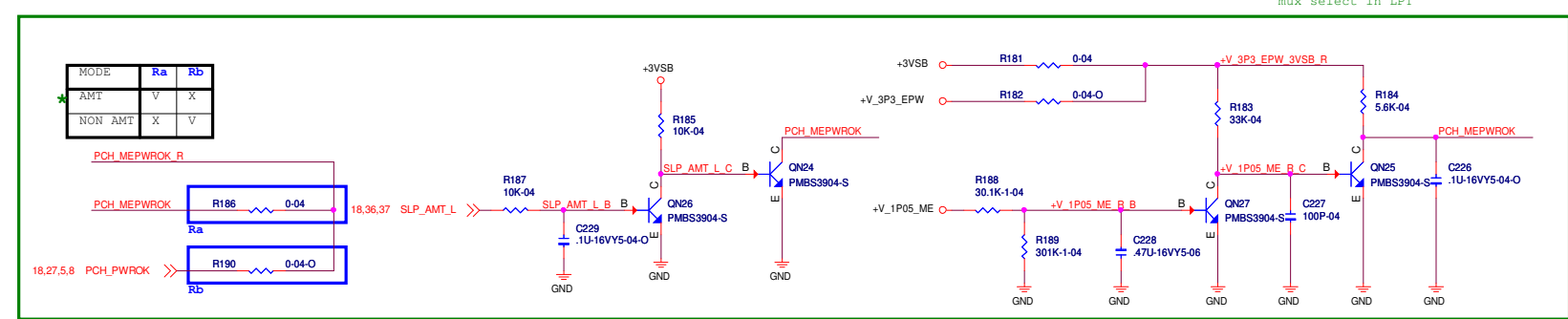
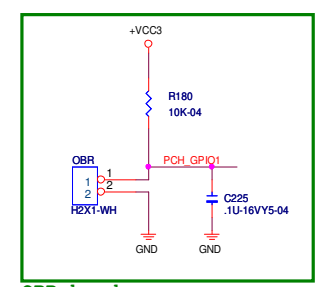
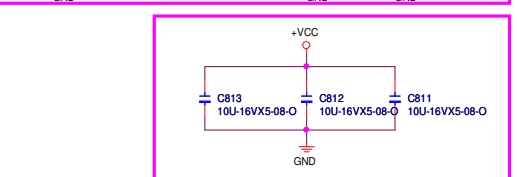
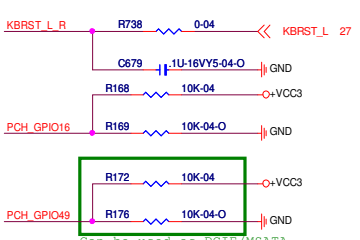
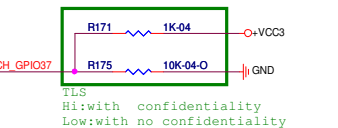
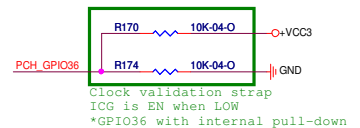
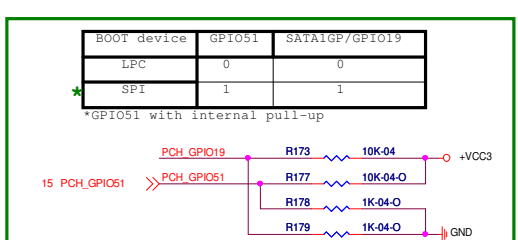
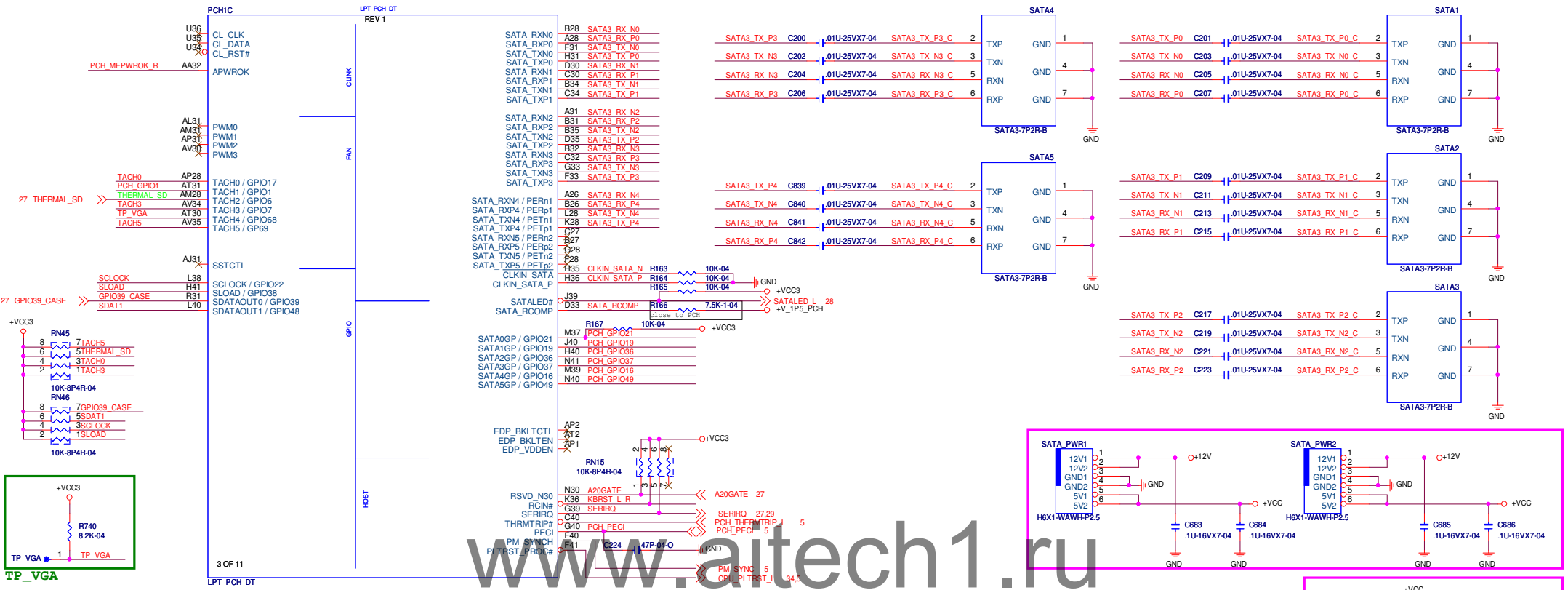


stitching caps for PCI\_CLK2\_FB

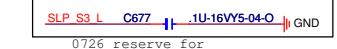
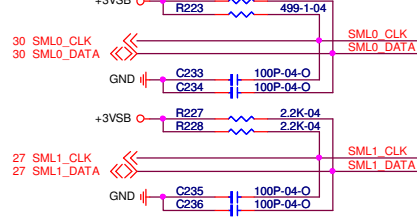
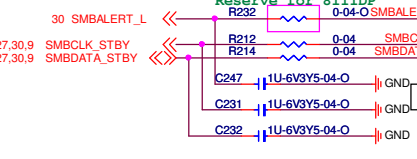
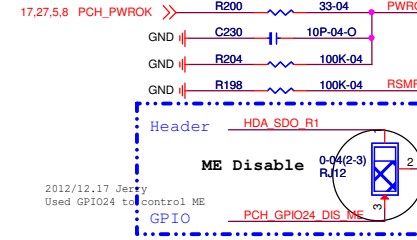
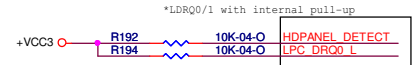


stitching caps for PEX16\_100M



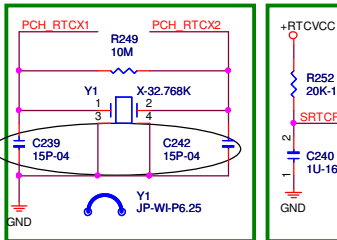
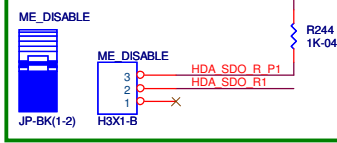


ME PWROK control circuit

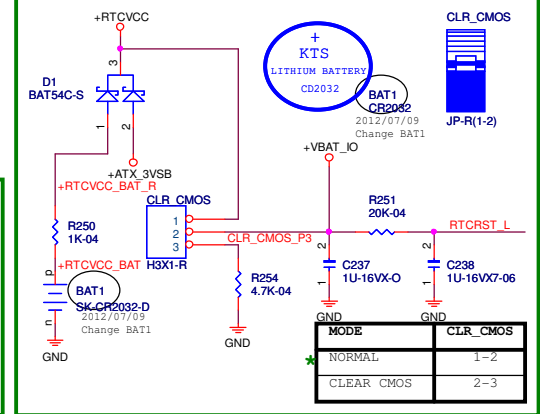


Disable ME Jumper	
MODE	SPI override
Disable ME	2-3
NORMAL	1-2

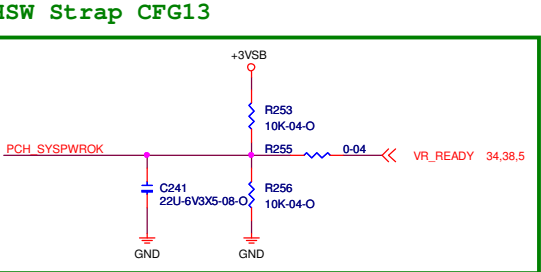
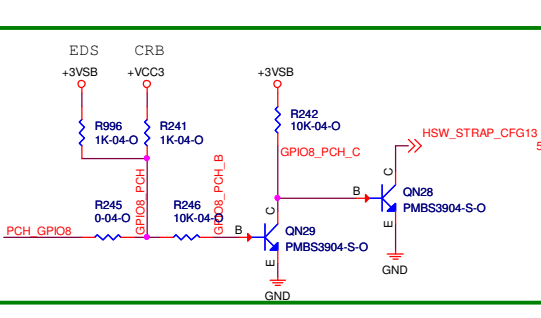
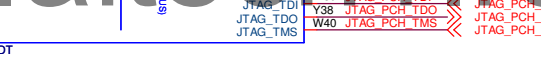
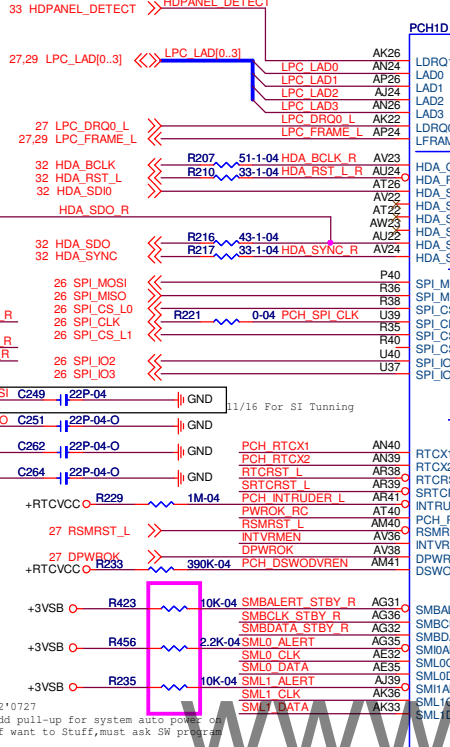
\*HDA\_SDO with internal pull-down



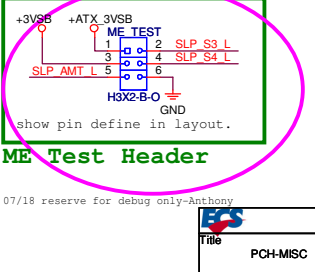
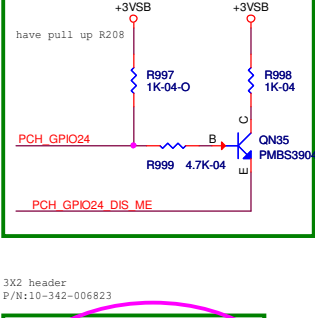
PCH Xtal 12\*0528  
C239 - C242 change to 15P for RTC test.



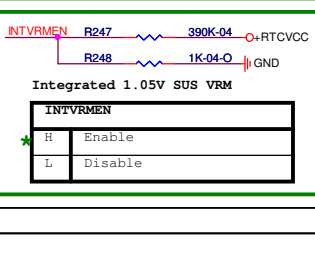
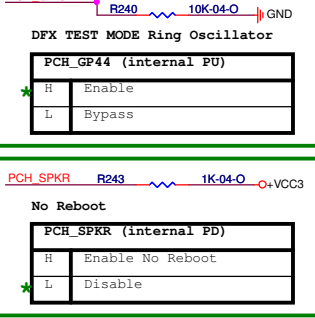
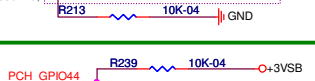
CLR\_CMOS 12\*0528  
C239 - C242 change to 15P for RTC test.



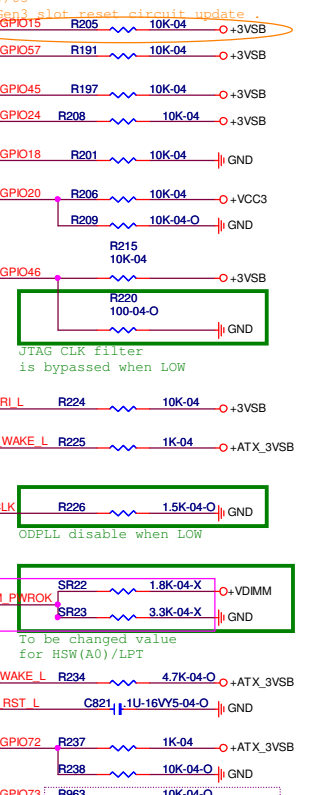
HSW Strap CFG13 12\*0528  
C239 - C242 change to 15P for RTC test.



ME Test Header 12\*0528  
C239 - C242 change to 15P for RTC test.



PCH\_GPIO24 12\*0528  
C239 - C242 change to 15P for RTC test.



2012/07/05  
PCH\_GPIO0 to PCH\_GPIO24 circuit update

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PCH\_GPIO0 to PCH\_GPIO24 circuit update

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2012/07/05  
PCH\_GPIO0 to PCH\_GPIO24 circuit update

2012/07/05  
PCH\_GPIO0 to PCH\_GPIO24 circuit update

2012/07/05  
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PCH\_GPIO0 to PCH\_GPIO24 circuit update

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PCH\_GPIO0 to PCH\_GPIO24 circuit update

2012/07/05  
PCH\_GPIO0 to PCH\_GPIO24 circuit update

2012/07/05  
PCH\_GPIO0 to PCH\_GPIO24 circuit update

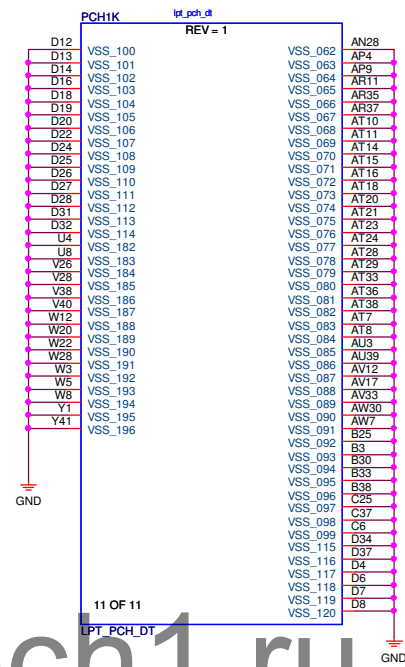
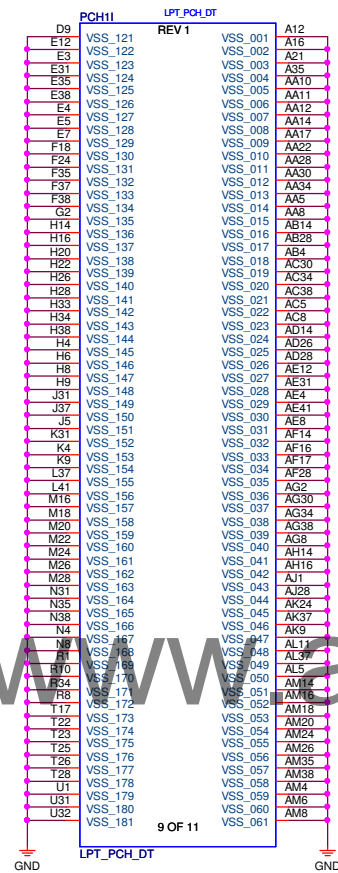
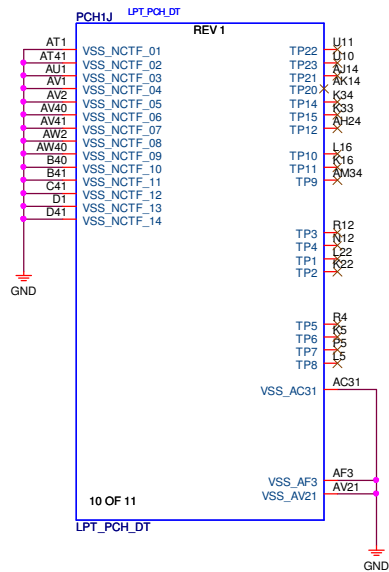
2012/07/05  
PCH\_GPIO0 to PCH\_GPIO24 circuit update

2012/07/05  
PCH\_GPIO0 to PCH\_GPIO24 circuit update

2012/07/05  
PCH\_GPIO0 to PCH\_GPIO24 circuit update

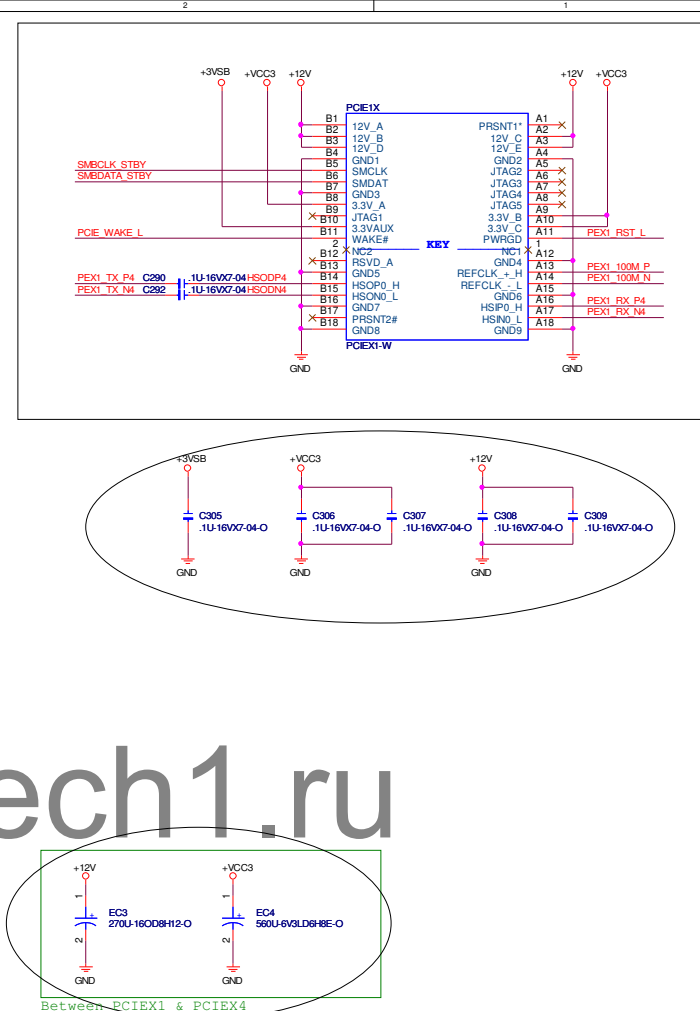
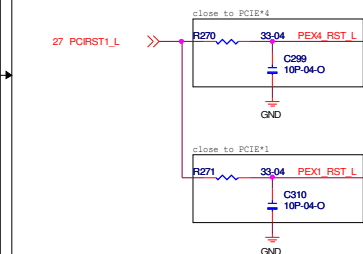




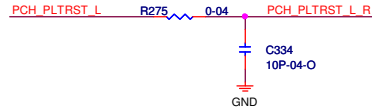


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23 AD[31:0] << AD[31:0]  
 23 C\_BE\_L[3:0] << C\_BE\_L[3:0]  
 23 PM66EN << PM66EN  
 23 FRAME\_L << FRAME\_L  
 23 IRDY\_L << IRDY\_L  
 23 TRDY\_L << TRDY\_L  
 23 STOP\_L << STOP\_L  
 23 DEVSEL\_L << DEVSEL\_L  
 23 PAR << PAR  
 23 SERR\_L << SERR\_L  
 23 PERR\_L << PERR\_L  
 23 LOCK\_L << LOCK\_L  
 23 PCICLK0 << PCICLK0  
 23 INTA\_L << INTA\_L  
 23 INTB\_L << INTB\_L  
 23 INTC\_L << INTC\_L  
 23 INTD\_L << INTD\_L  
 23 REQ0\_L << REQ0\_L  
 23 GNT0\_L << GNT0\_L  
 23 PCIRST\_L << PCIRST\_L

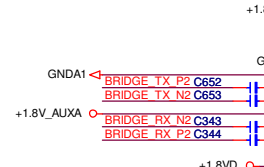


15,27,30 PCH\_PLTRST\_L << PCH\_PLTRST\_L

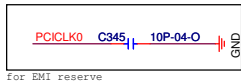
PCH=>

15 BRIDGE\_TX\_P2 << BRIDGE\_TX\_P2  
 15 BRIDGE\_TX\_N2 << BRIDGE\_TX\_N2  
 15 BRIDGE\_RX\_P2 << BRIDGE\_RX\_P2  
 15 BRIDGE\_RX\_N2 << BRIDGE\_RX\_N2  
 16 BRIDGE\_100M\_N << BRIDGE\_100M\_N  
 16 BRIDGE\_100M\_P << BRIDGE\_100M\_P

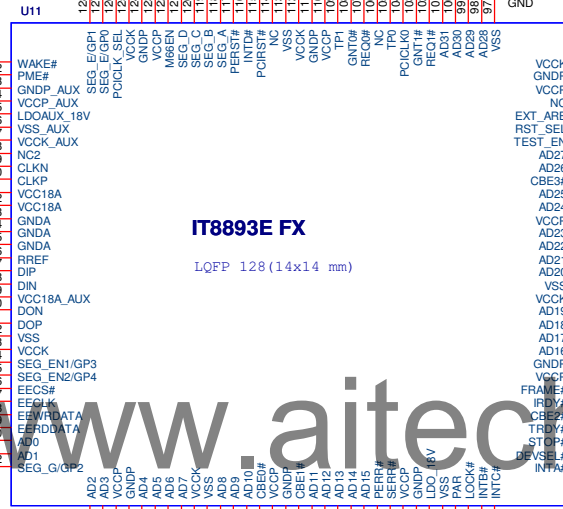
+3VSB  
 +1.8V\_AUXA  
 +1.8V\_AUXD



BRIDGE\_100M\_N R280 0-04 BRIDGE\_CLK\_N  
 BRIDGE\_100M\_P R281 0-04 BRIDGE\_CLK\_P

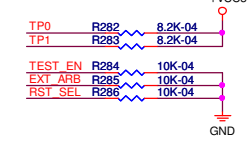
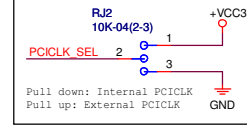
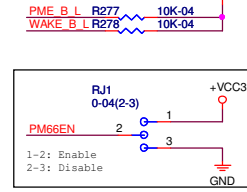
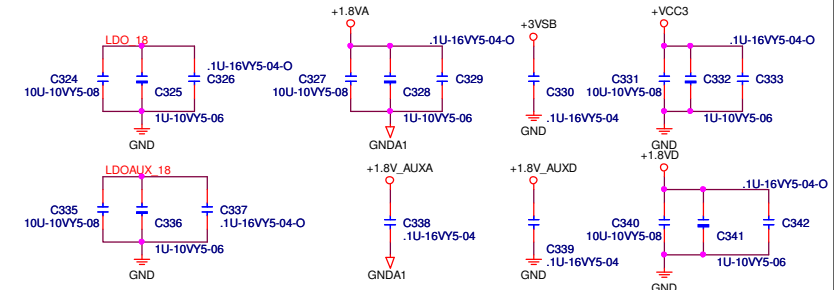


For EMI reserve

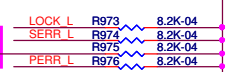
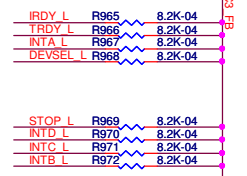


IT8893E FX

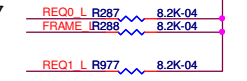
LQFP 128(14x14 mm)



PCI BUS 5V external pull up 2.7Kohm  
 PCI BUS 3.3V external pull up 8.2Kohm



0726 Add pull up for ITE review-Anthony



PCIE CLK PCB layout note:  
 To meet Differential Impedance :100 ohm +/- 15%  
 To meet Single-ended Impedance :50 ohm +/- 15%  
 CLKP and CLKN trace width:7 mils  
 Space between CLKP and CLKN:14 mils  
 L1 & L2 height:5 mils  
 The signal traces Number of vias: 4 (Max.)  
 The signal trace above analog GND plane  
 Spacing from other groups:>25 mils  
 Total trace length: 12 inches (Max.)  
 The size of R4;R5 is "0402"  
 The size of R6;R7 is "0402"

PCIE DIP;DIN;DOP;DON PCB layout note:  
 To meet Differential Impedance :85 ohm +/- 15%  
 To meet Single-ended Impedance :50 ohm +/- 15%  
 PCIE DIP and DIN trace width:9.5 mils  
 PCIE DOP and DON trace width:9.5 mils  
 Space between DIP/DIN and DOP/DON:14.5 mils  
 L1 & L2 height:5 mils  
 The signal traces Number of vias: 2 (Max.)  
 The signal trace above analog GND plane  
 Spacing from other groups:>25 mils  
 Total trace length: 12 inches (Max.)  
 The size of C24;C25 is "0402"

22 AD[31..0] <<> AD[31..0]  
 22 C\_BE\_L[3..0] <<> C\_BE\_L[3..0]

22 GNT0\_L <<> GNT0\_L  
 22 REQ0\_L <<> REQ0\_L

22 INTA\_L <<> INTA\_L  
 22 INTB\_L <<> INTB\_L  
 22 INTC\_L <<> INTC\_L  
 22 INTD\_L <<> INTD\_L

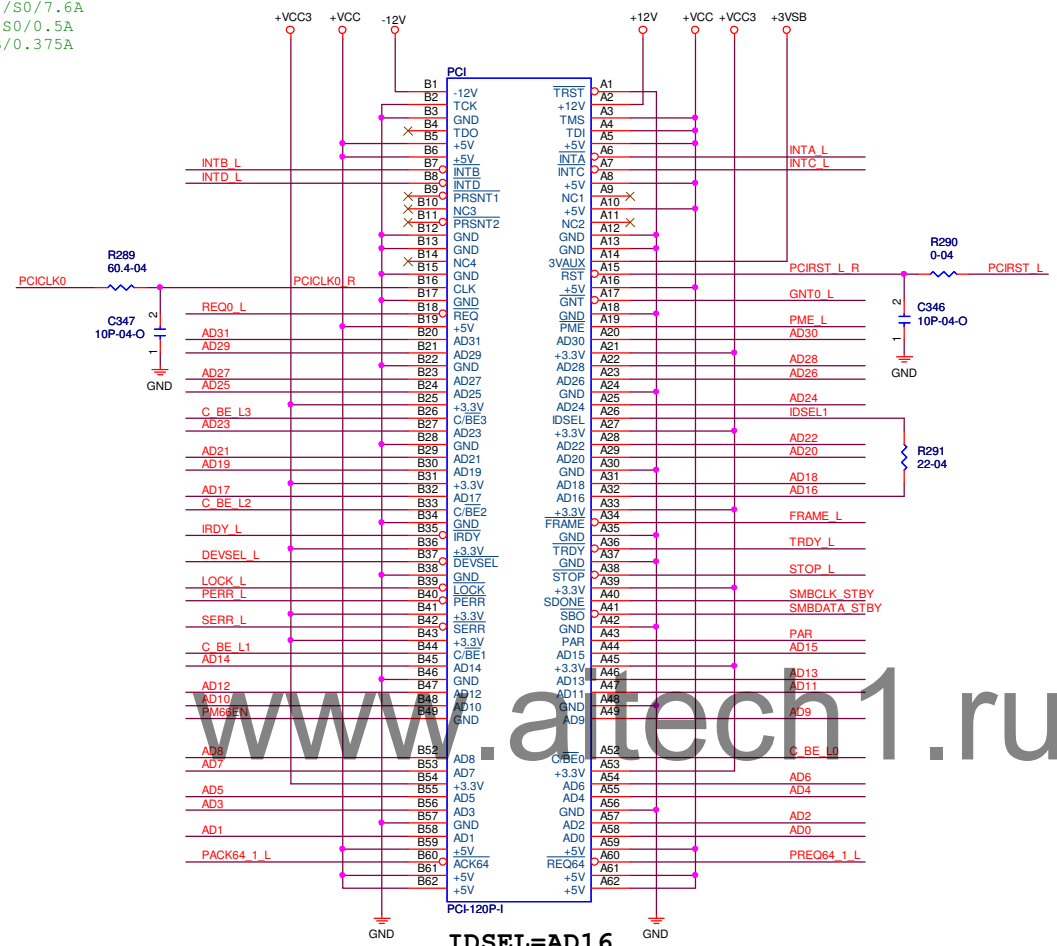
22 PAR <<> PAR  
 22 DEVSEL\_L <<> DEVSEL\_L  
 22 IRDY\_L <<> IRDY\_L  
 15 PME\_L <<> PME\_L  
 22 SERR\_L <<> SERR\_L  
 22 STOP\_L <<> STOP\_L  
 22 LOCK\_L <<> LOCK\_L  
 22 TRDY\_L <<> TRDY\_L  
 22 PERR\_L <<> PERR\_L  
 22 FRAME\_L <<> FRAME\_L

22 PCIRST\_L <<> PCIRST\_L  
 22 PCICLK0 <<> PCICLK0  
 22 PM66EN <<> PM66EN

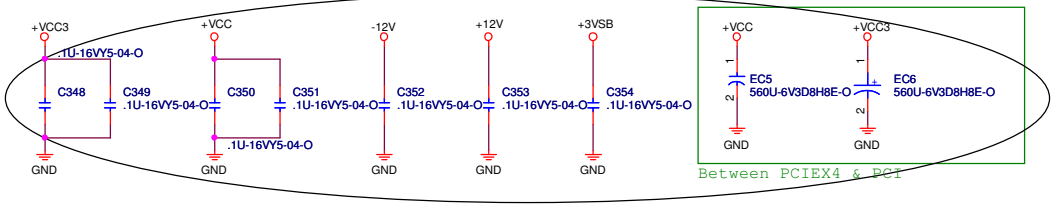
18,21,26,27,30,9 SMBCLK\_STBY <<> SMBCLK\_STBY  
 18,21,26,27,30,9 SMBDATA\_STBY <<> SMBDATA\_STBY

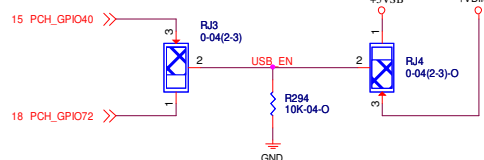
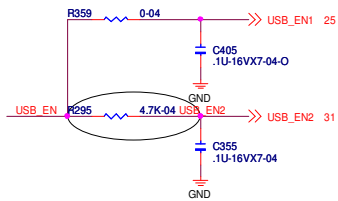
\*\*PCI Slot\*\*  
 +VCC/S0/5A  
 +VCC3/S0/7.6A  
 +V12/S0/0.5A  
 +3VSB/0.375A

+VCC3 R292 8.2K-04 PACK64\_1\_L  
 R293 8.2K-04 PREQ64\_1\_L

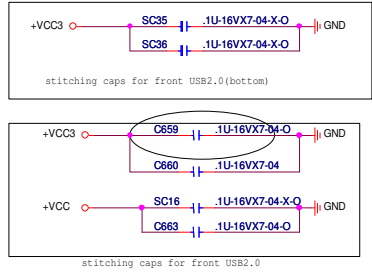


IDSEL=AD16  
 INT[A,B,C,D]





	uP7536 Enable use	RJ?	RJ?	S4/S5 USB_5V_DUAL	Customer
	VDIMM	0ohm (1-2)	NA	0 Volt	Acer S4 w/o S5 w/ USB_5VDUAL
	5VSB	0ohm (2-3)	NA	5 Volt	
*	GPIO	NA	0 ohm	S4 : 0 Volt S5 : 5 Volt	

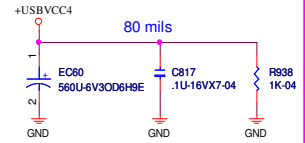
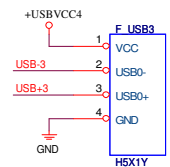
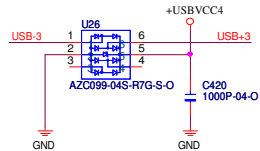
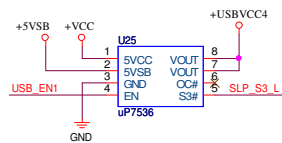


Footprint: CMM21\_R0402

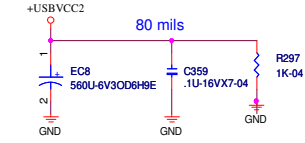
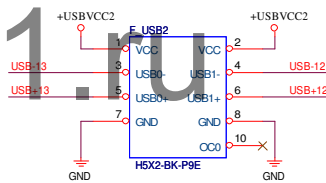
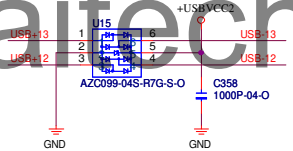
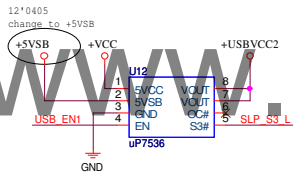
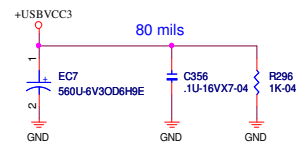
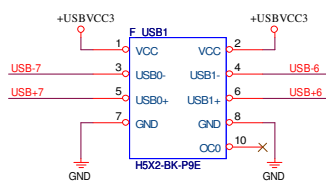
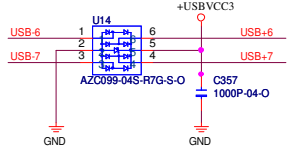
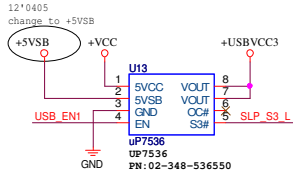
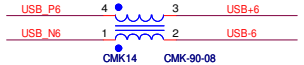
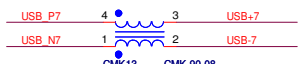
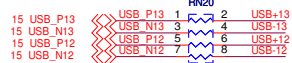
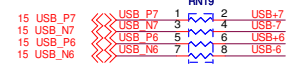


default上電阻, 位置為 CMK37 (1-2), CMK37 (3-4)

V.B 上 Choke

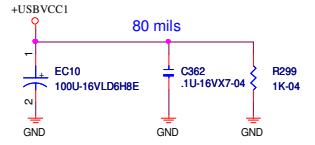
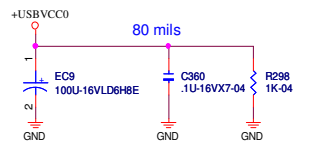
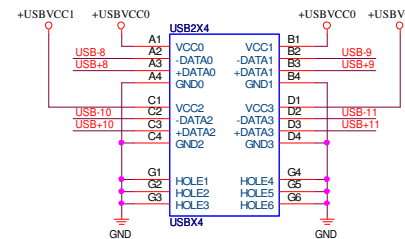
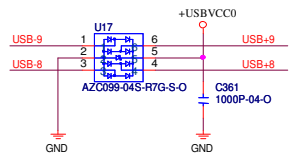
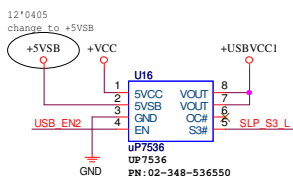
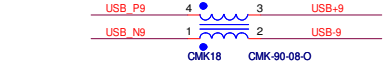
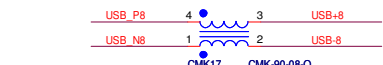
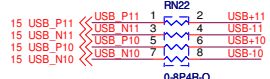
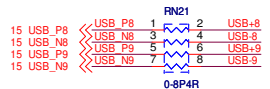


18,19,25,27,31,36,37,5 SLP\_S3\_L >> SLP\_S3\_L

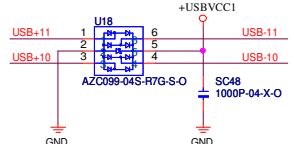


USB2.0 header

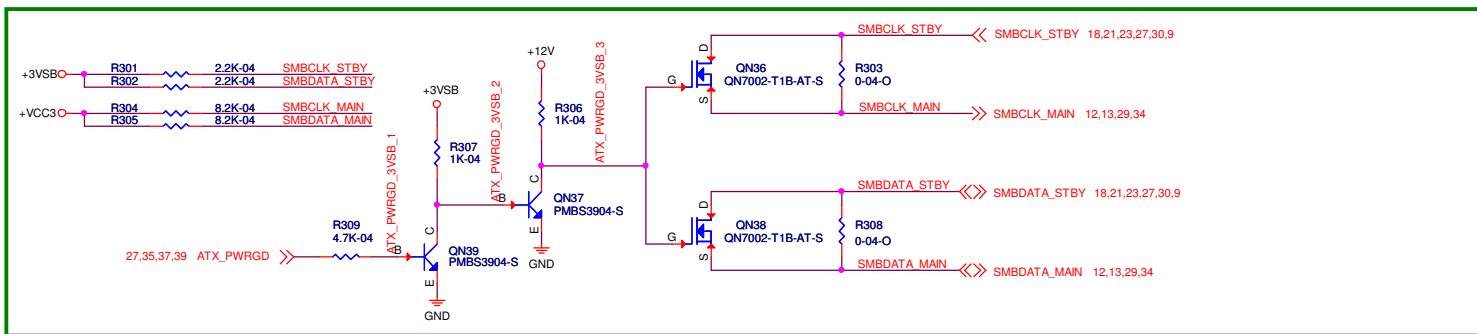
USB2.0 connector



- OC[3:0]# should be connected with USB 2.0 ports 0 - 7 and any 4 of USB 3.0 ports 1 - 6.
- OC[7:4]# should be connected with USB 2.0 ports 8 - 13 and any 4 of USB 3.0 ports 1 - 6.

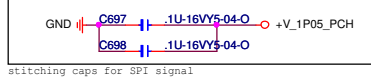
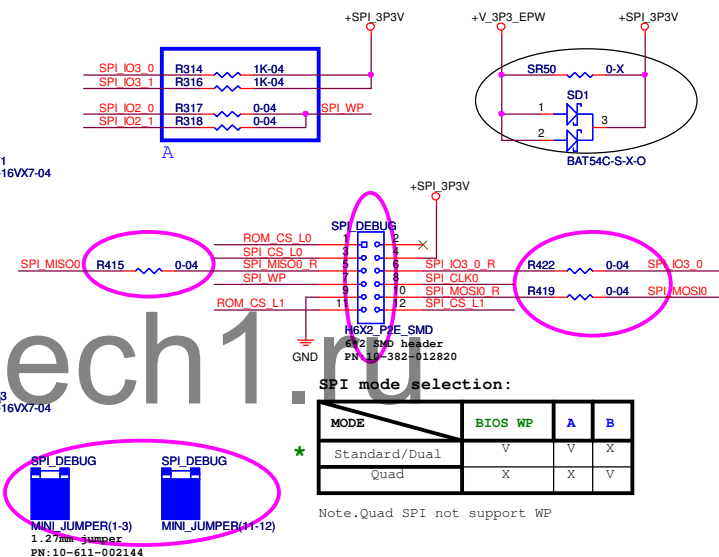
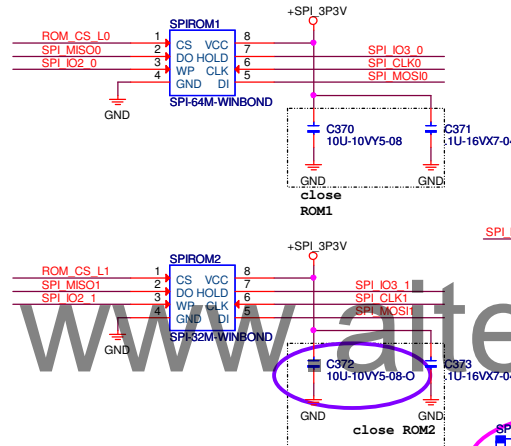
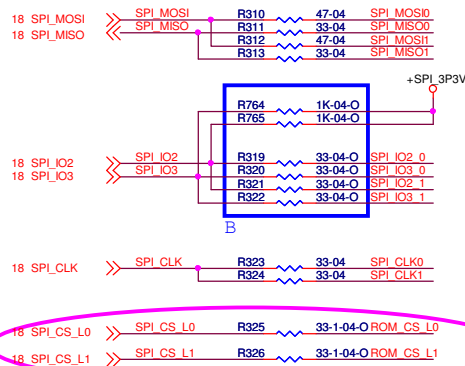






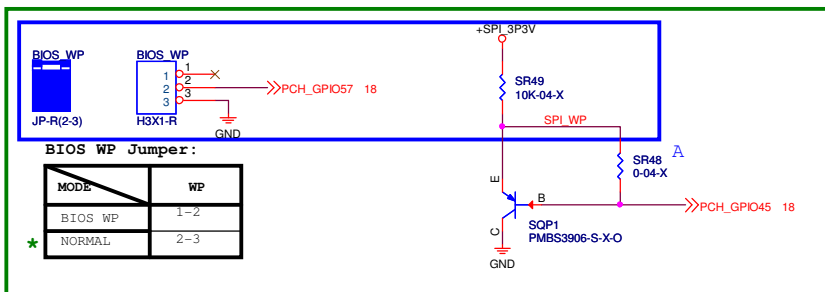
SMBus Logic Circuit

2013'03'20  
unstuff S01 change to SR50 for SPI Dubug board



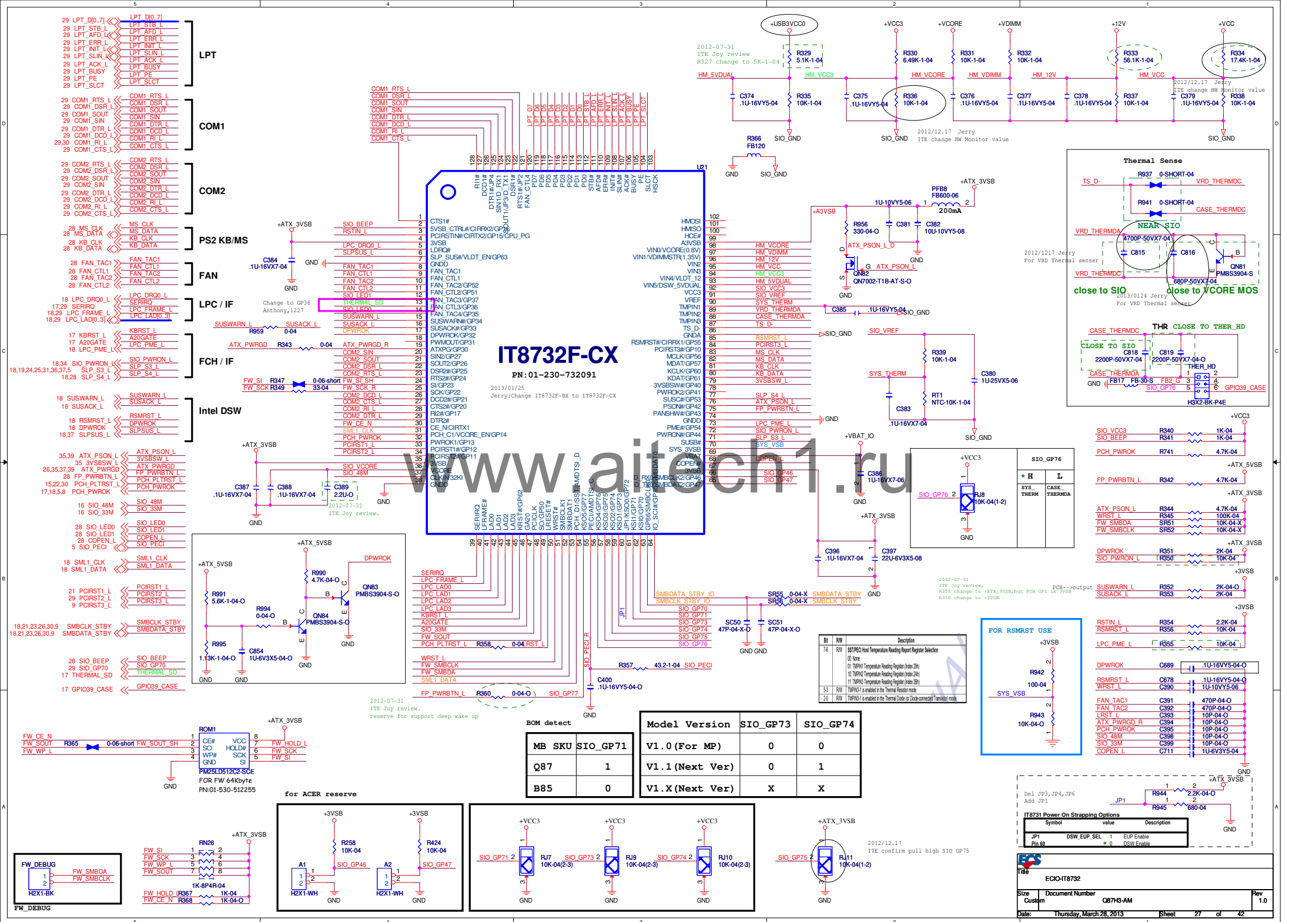
stitching caps for SPI signal

## SPI ROM

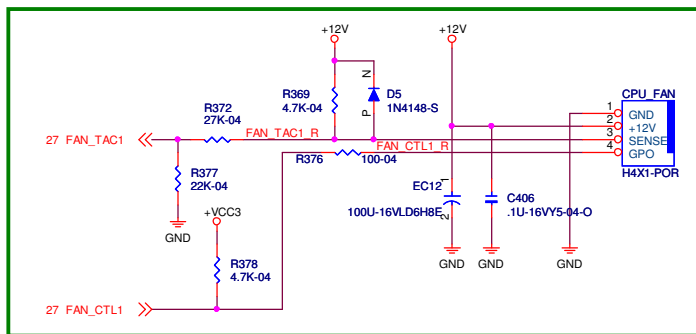


## BIOS WP

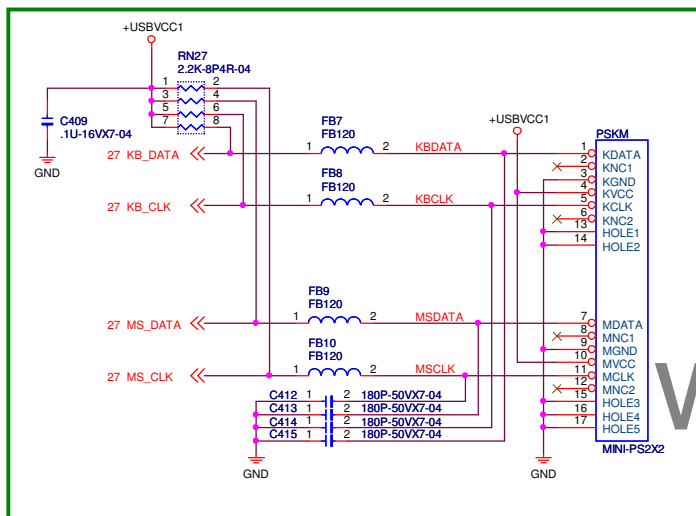
07/18 reserve for debug only-Anthony



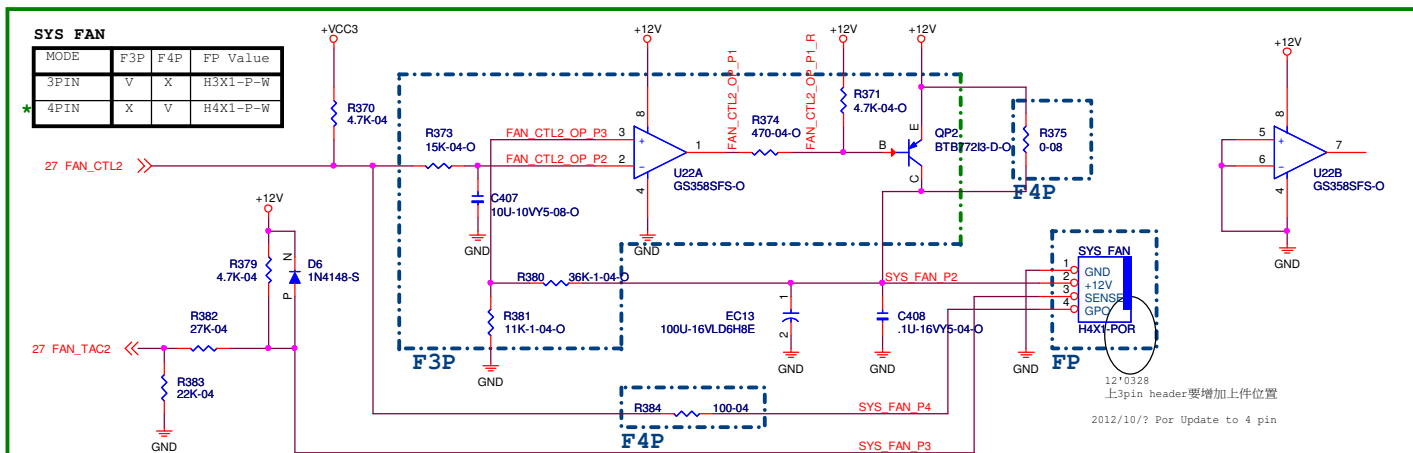




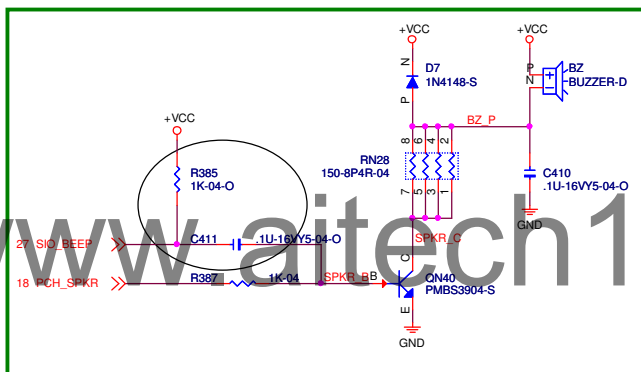
CPU\_FAN 4 pin circuit



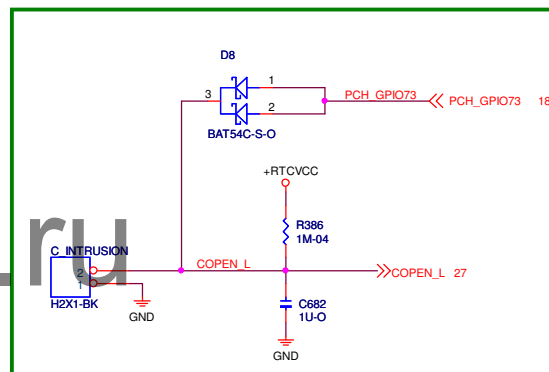
PS2 circuit



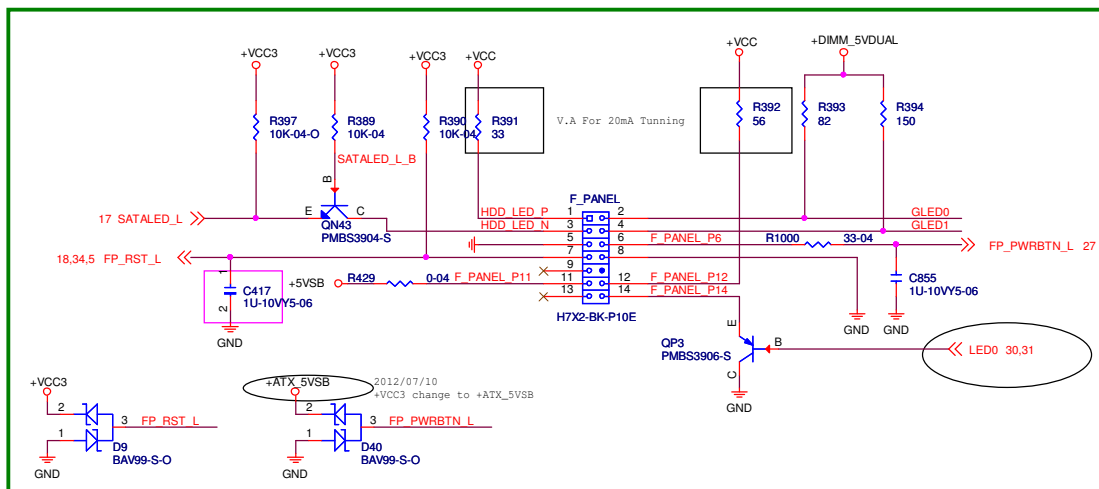
SYS\_FAN 3/4 pin co-layout circuit



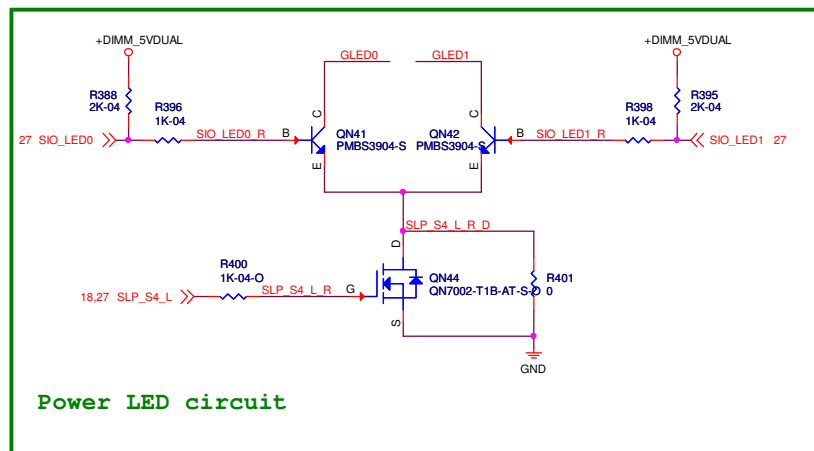
Buzzer circuit



Case open circuit




Front Panel circuit



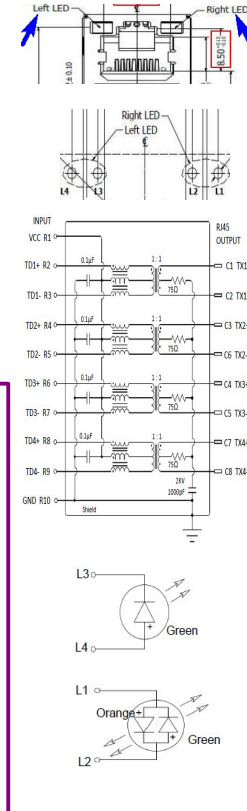
Power LED circuit

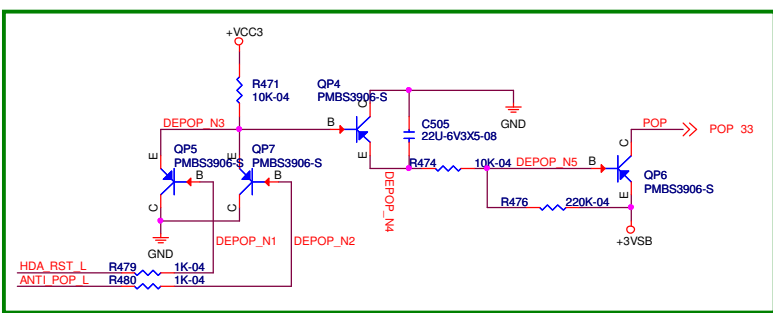




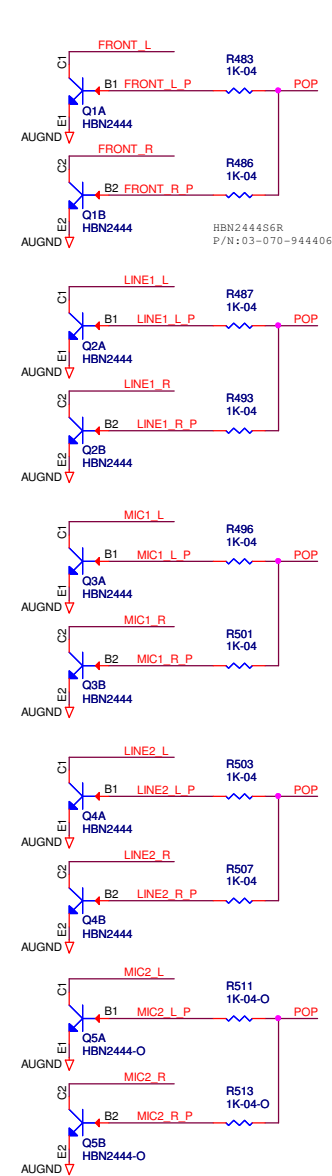
			
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LPT/COM/TPM			
Size	Document Number		Rev
Custom	O67H3-AM		1.0
Date:	Thursday, March 28, 2013	Sheet	29 of 42

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LAN Intel & Realtek			
Size	Custom	Document Number	Rev
		Q87H3-AM	1.0
Date:	Thursday, March 28, 2013		Sheet 30 of 42

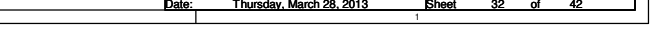
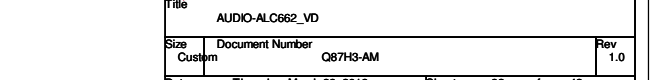
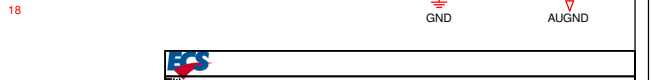
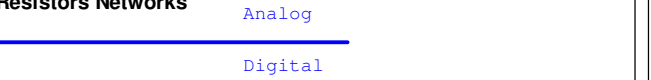
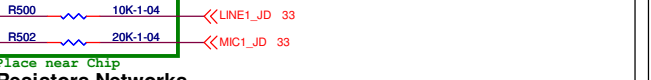
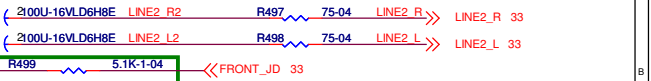
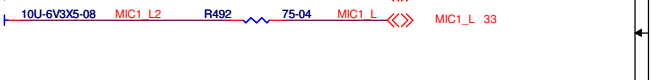
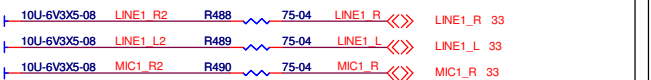
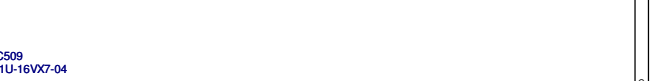
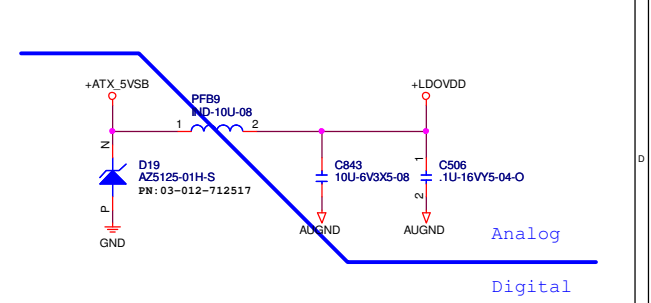
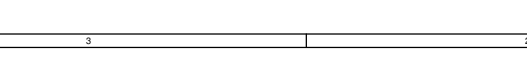
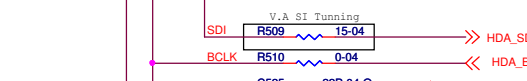
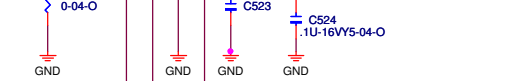
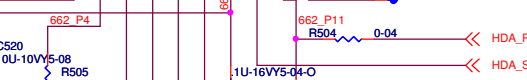
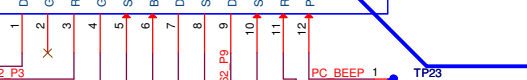
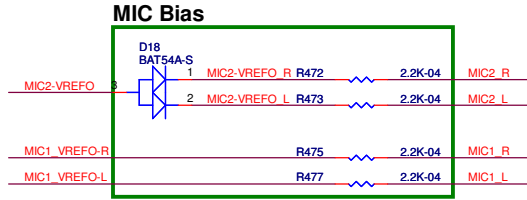
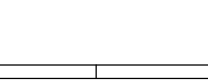
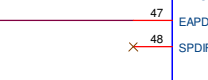
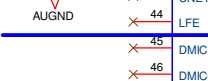
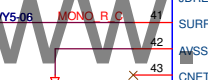
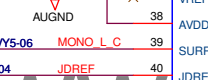
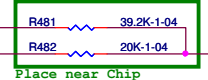




De-pop circuit

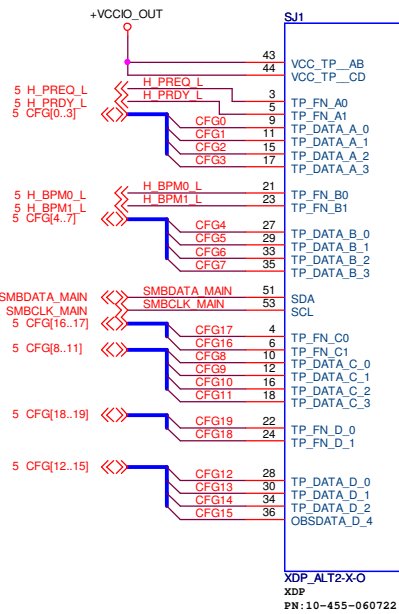
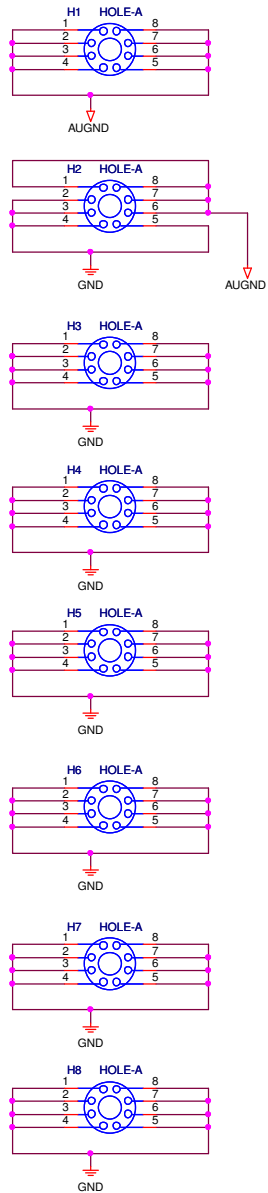


### Resistors Networks



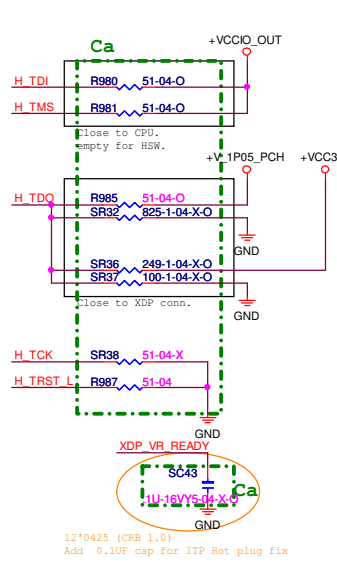
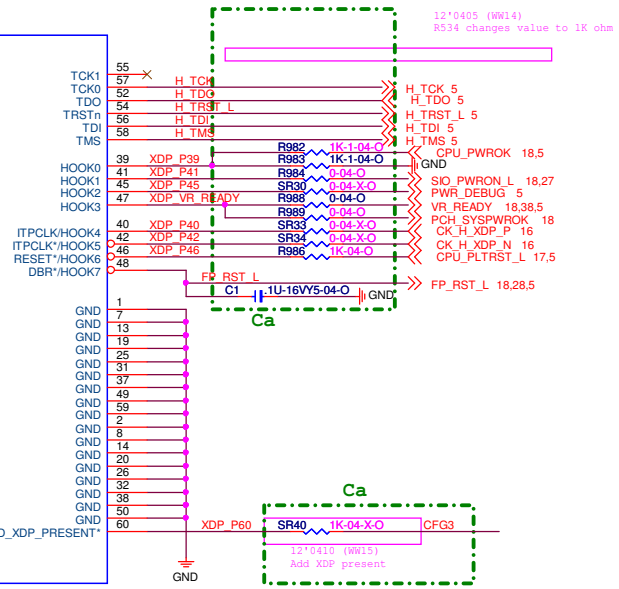
Title			AUDIO-ALC662_VD
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Custom			
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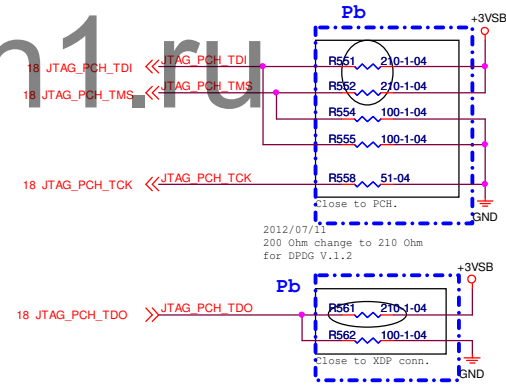
XDP  
PN:10-455-060722

www.aitech1.ru



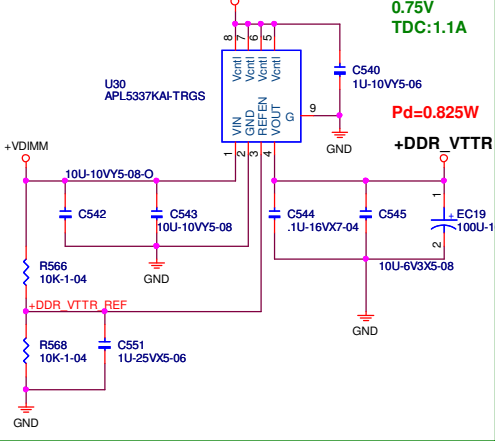
	Ca
CPU XDP function	V
NO CPU XDP function	X

-O:報價

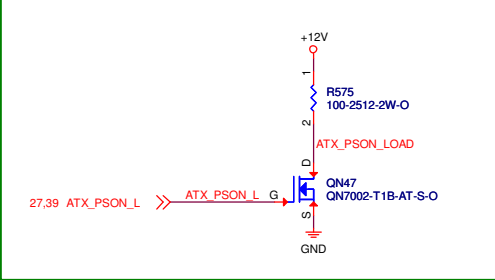


	Pb
PCH XDP function	V
NO PCH XDP function	X

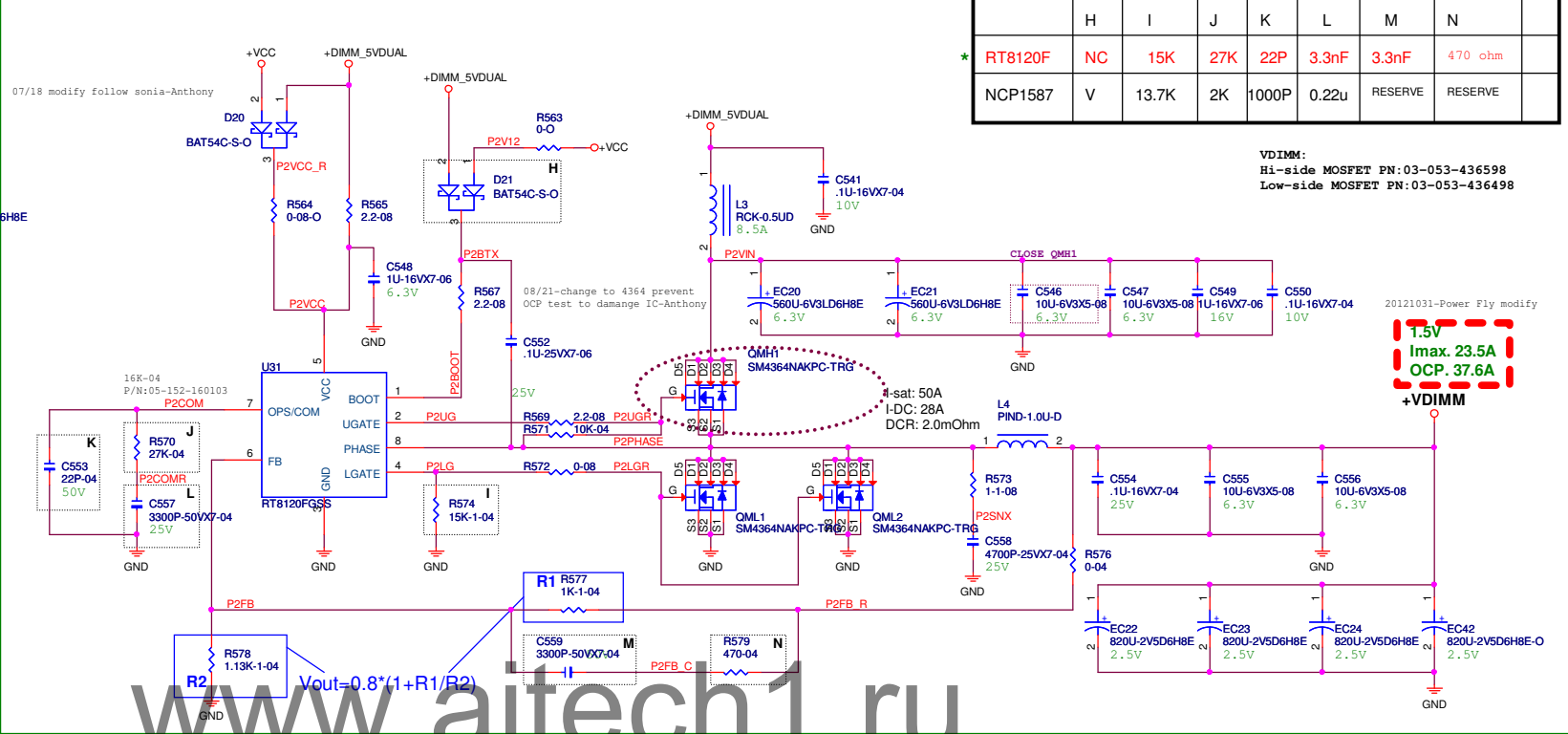
# DDR VTT



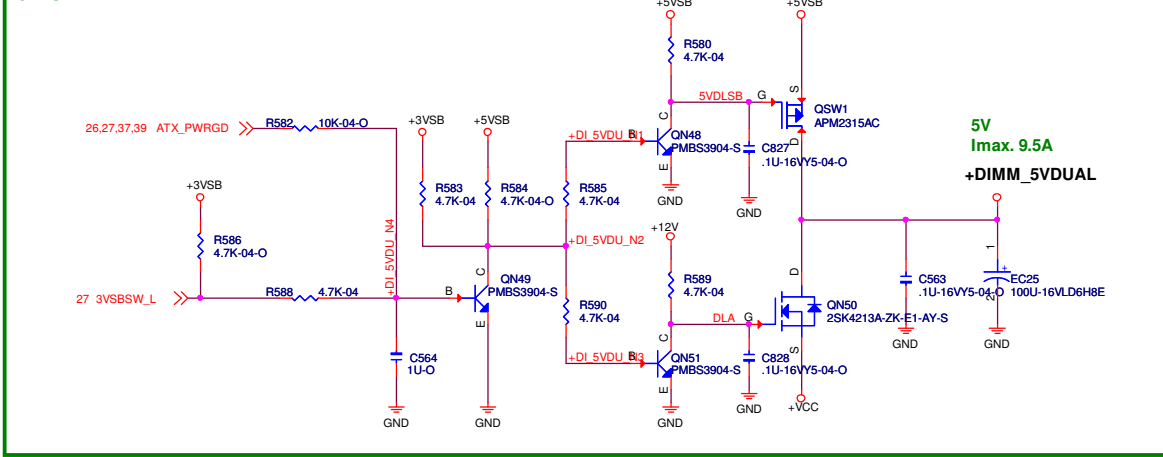
# Dummy Load for ATX power



# VDIMM



# 5VDUAL

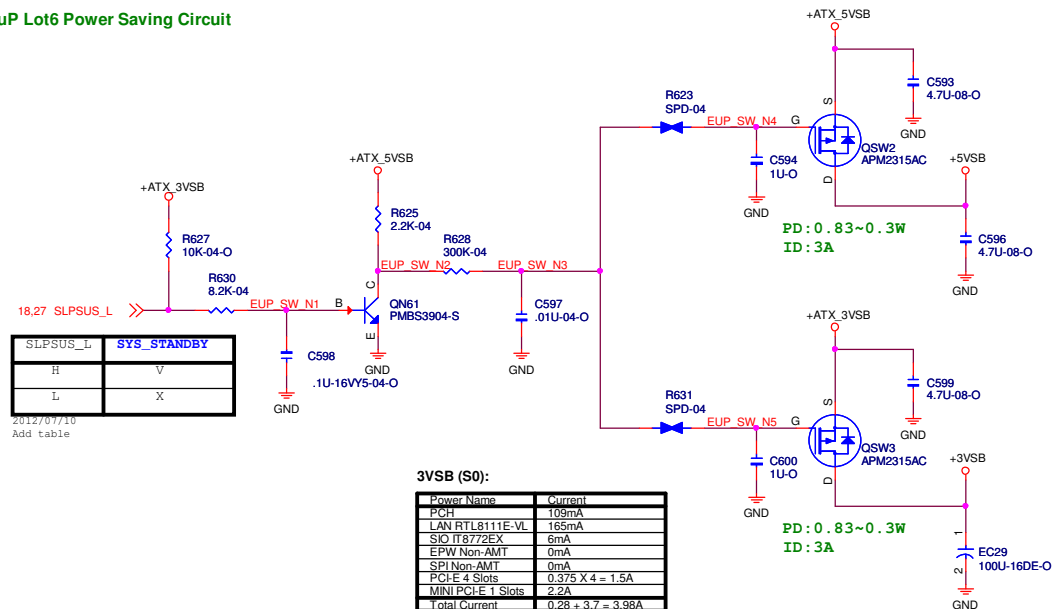




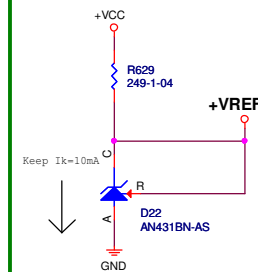
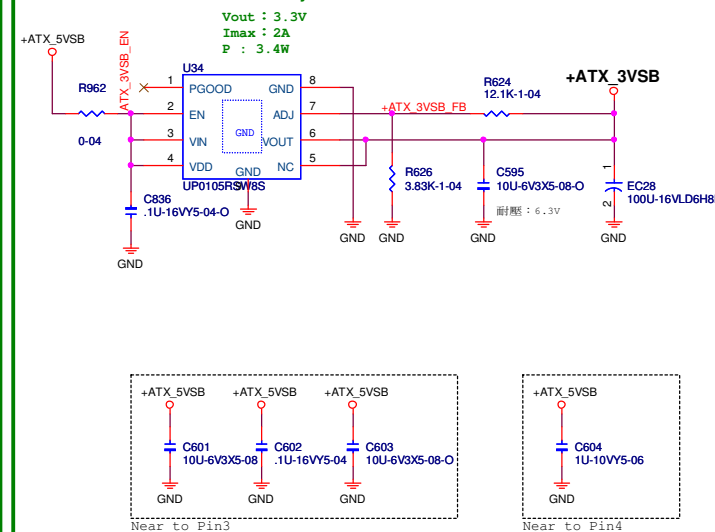




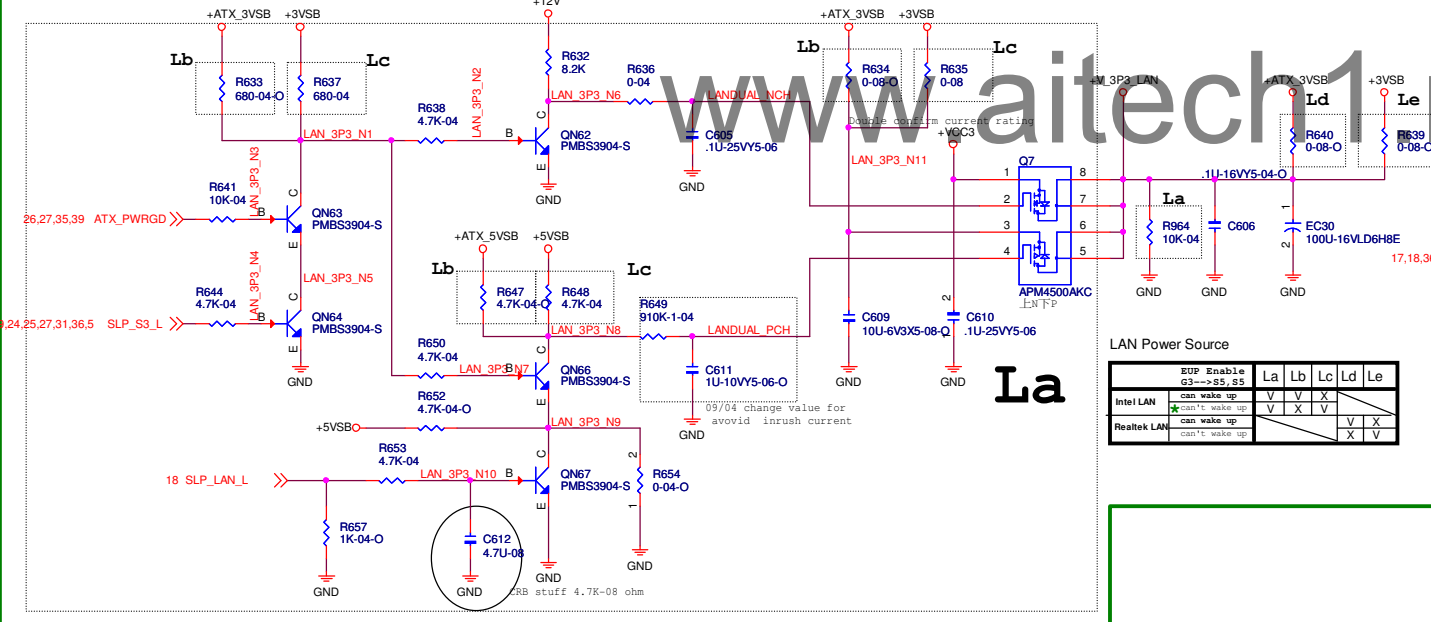
## EuP Lot6 Power Saving Circuit



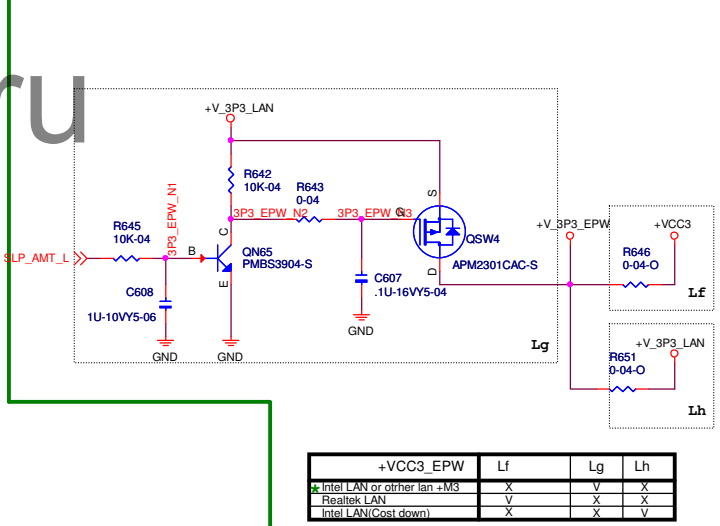
## +3V Standby



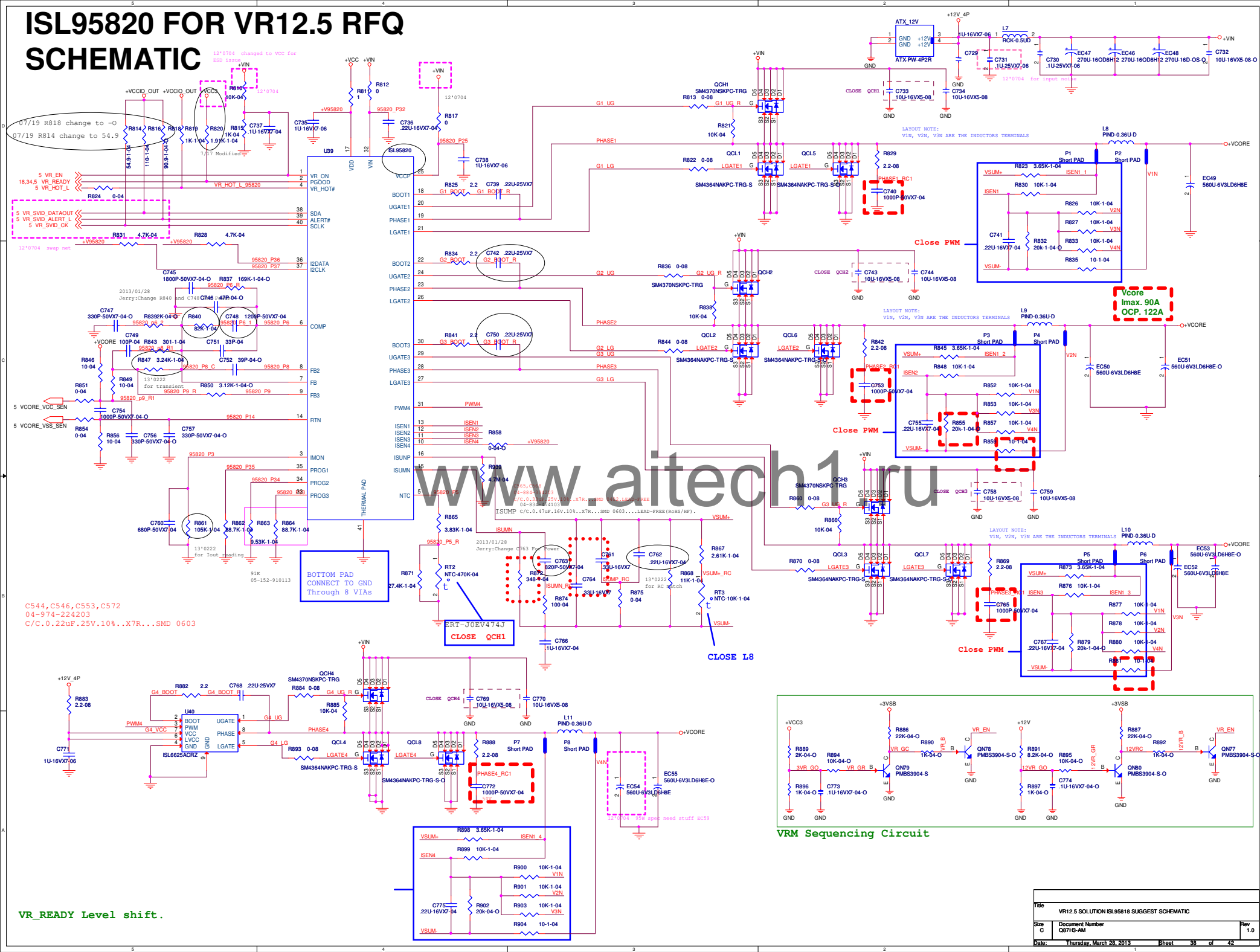
## LAN Power Circuit



## SPI ROM & PCH Power Circuit



# ISL95820 FOR VR12.5 RFQ SCHEMATIC



VR\_READY Level shift.

### VRM Sequencing Circuit

Title				
VR12.5 SOLUTION ISL95818 SUGGEST SCHEMATIC				
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